CMS Muon Trigger Meeting **11.03.1996**

Muon Trigger Milestones

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D300	96 Nov	Review of test benches with FPGA prototypes of PAC and synchro/ readout chips (Warsaw)
D310	96 Nov	Review of FPGA prototype tests of the muon sorter ASIC (Bari)
D320	96 Nov	Review of FPGA prototype tests of the meantimer ASIC (Padova)
D330	96 Nov	Review of FPGA prototype tests of the Track Finder ASIC's (Vienna)
D340	96 Nov	Delivery of prototypes of comparator tree and pattern finding chips for cathode strip chamber trigger (UCLA, MIT, CERN)
D350	97 Jun	Delivery of first presamples of PAC, synchro/readout and sorter ASIC's (Warsaw, Bari)
D360	97 Jun	Delivery of prototypes of wire pattern-finding and bunch i.d. chips for CSC trigger (UCLA, CMU, OSU)
D370	97 Nov	Delivery of first presamples of ASICs for strip and wire LCT generation for CSC trigger (UCLA, UCD, OSU)
D380	97 Nov	Review of prototype design of motherboard circuits for CSC trigger (UCLA, UCD, OSU, Dubna)
D390	97 Dec	Delivery of meantimer and correlator final chips for full trigger test (Padova) =M16
D341	97 Dec	Prototype tests of center cluster and pattern finding chips for MF1/1 trigger (Dubna)
D361	97 Dec	Prototype tests of wire bunch i.d. and pattern finding chips for MF1/1 trigger (Dubna)

D300 96 Nov ***Review of test benches with FPGA prototypes of PAC and synchro/ readout chips (Warsaw)***

The test bench of the Pattern Comparator Trigger for RPC will consist of 4 cards: synchronisation, trigger, readout, and control. They will be equipped with FPGA versions of the Pattern Comparator (PAC) chip and the synchronisation module. The RD6 ROC ASIC will be used for the readout. The primary purpose is to test the system aspects of the complete muon trigger setup. The setup will be equipped with boundary scan, which will be used for testing and programming. The modular structure of the test bench will allow for changes from FPGA's to ASIC's once the latter are available (D350).

D310 96 Nov ***Review of FPGA prototype tests of the muon sorter ASIC (Bari)***

The muon sorter selects 4 highest momentum muons in the entire muon trigger system. It is a tree-like structure of sorter chips, each one selecting 4 out of 8 muons. FPGA versions of this chip will be tested in the test bench (D300).

D350 97 Jun ***Delivery of first presamples of PAC, synchro/readout and sorter ASIC's (Warsaw, Bari)***

These ASIC's will have full functionality but the size (number of channels) may be smaller than in the final versions. They will replace corresponding FPGA prototypes and the RD6 ROC ASIC in the test bench (D30 and D31). The technology for the prototype ASICS will be 0.7 um, whereas the final version is planned to be 0.35 um.

D320 96 Nov ***Review of FPGA prototype tests of the meantimer ASIC (Padova)***

Three meantimer prototypes in a FPGA reduced version, mounted on a 6U VME card, have been tested on H2 beam in summer '95. Detailed analysis of their performance will be completed

D390 97 Nov ***Delivery of meantimer and correlator final chips for full trigger test (Padova) =M16***

The final meantimer and correlator chips will be mounted on 128 channel Trigger Boards connected to MB97 chamber (end '97 milestone). Trigger Boards will be mounted in a 9U VME crate with a dedicated backplane, along with a Control Board, to test the full chain of chamber triggering devices.

D330 96 Nov ***Review of FPGA prototype tests of the Track Finder ASIC's (Vienna)***

The hardware implementation of the track finder is going to be tested using a FPGA prototype system. In the first testing phase the chamber electronics will not be available, thus the track finder prototype will be evaluated in a prototype test bench. This test bench will deliver simulated physics data to the FGPA prototype.

D340 96 Nov ***Delivery of prototypes of comparator tree and pattern finding chips for cathode strip chamber trigger (UCLA, MIT, CERN)***

The CSC chamber strip preamp/fast shaper ASICs plus strip comparator tree ASICs plus strip pattern-finding FPGAs will be connected to 16 strip x 6 layers of a CSC prototype chamber and tested for efficiency and spatial resolution.

D341 97 Dec ***Prototype tests of center cluster and pattern finding chips for MF1/1 trigger (Dubna)***

Cathode front end electronics based on Minsk ASICs (amp./shaper, fast shaper/Discr.) will be available in May 97. They will be mounted on the P3 prototype of MF1/1 together with center cluster and pattern finding FPGAs prototypes.

D360 97 Jun ***Delivery of prototypes of wire pattern-finding and bunch i.d. chips for CSC trigger (UCLA, CMU, OSU)***

The CSC wire preamp/discriminator ASICs plus wire pattern-finding/bunch i.d. FPGAs will be connected to 16 strips x 6 layers of a CSC prototype chamber and tested for efficiency, and time resolution.

D361 97 Dec ***Prototype tests of wire bunch i.d. and pattern finding chips for MF1/1 trigger (Dubna)***

Anode front end electronics based on Minsk ASICs (preamp./shaper, discr.) will be available in May 97. It will be mounted on the P3 prototype of MF1/1 together with wire pattern finding and BX identification FPGA prototypes.

D370 97 Nov ***Delivery of first presamples of ASICs for strip and wire LCT generation for CSC trigger (UCLA, UCD, OSU)***

The strip pattern-finding and wire pattern-finding/bunch i.d. trigger chips will be implemented in ASICs with intended performance close to final design specifications.

D380 97 Nov ***Review of prototype design of motherboard circuits for CSC trigger (UCLA, UCD, OSU, Dubna)***

Motherboard circuits will receive and correlate wire and strip trigger information and pass stub information on to the Track Finder (see D330) over an optical fiber.