D340: CSC Comparators & Pattern Arrays

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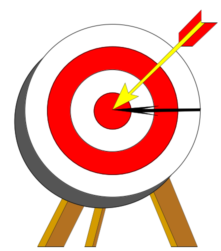
D340- 1996 Nov

Delivery of prototypes of comparator tree and pattern finding chips for cathode strip chamber trigger (UCLA,MIT,CERN)

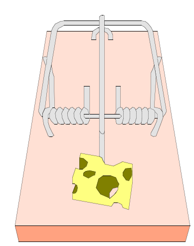
The CSC chamber strip preamp/fast shaper ASICs plus strip comparator tree ASICs plus strip pattern-finding FPGAs will be connected to 16 strip x 6 layers of a CSC prototype chamber and tested for efficiency and spatial resolution.

1) Beam Test of Comparators



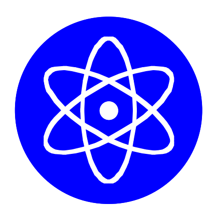
- Korytov test board, L. Gorn analysis
- Tests done on P0 chamber at CERN
- □□
- □□

2) Comparator ASIC, 8-ch version



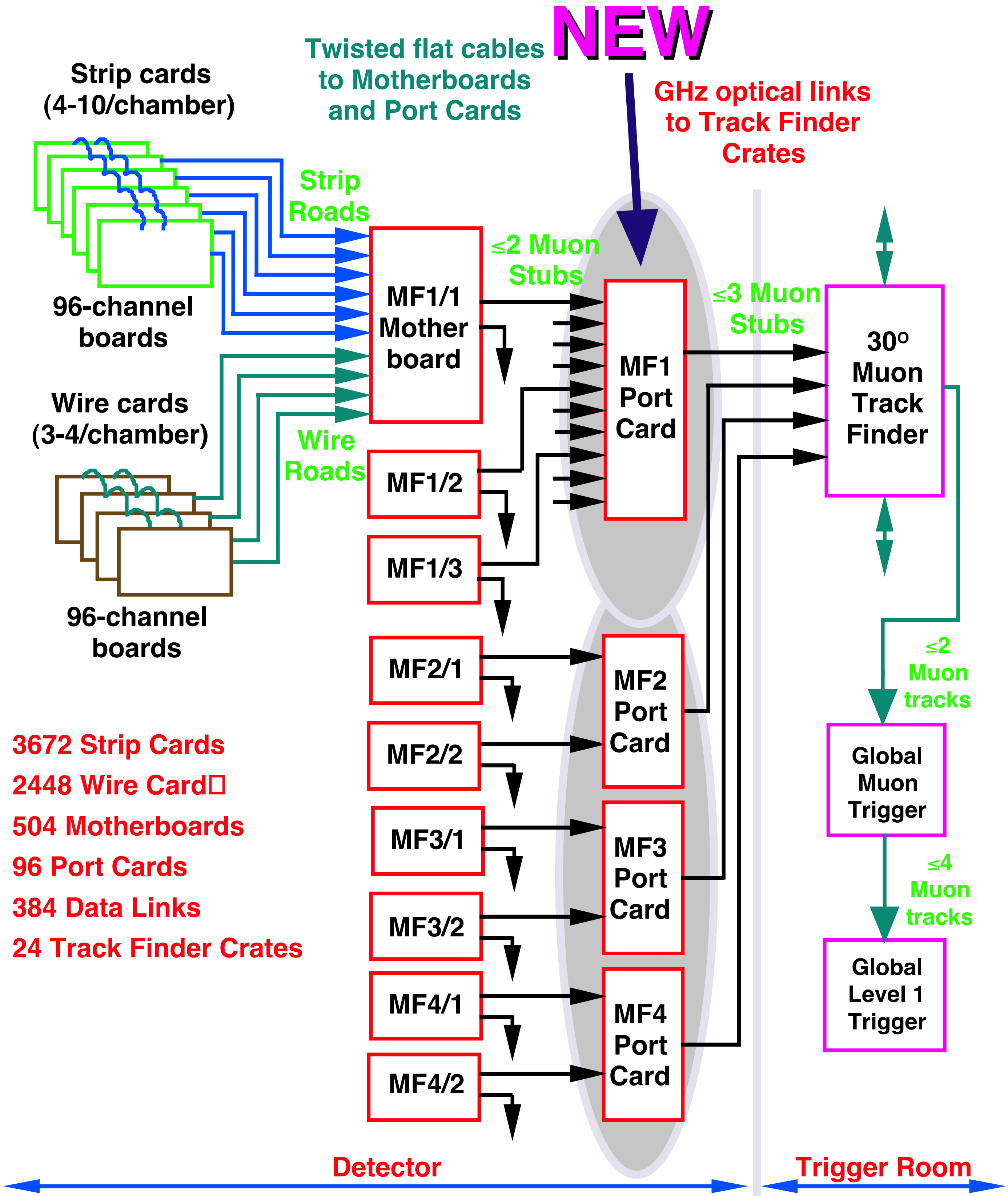
- J.-C. Santiard
- Layout done, chip delivery mid-Dec.
- □□
- □□

3) Pattern Array FPGA



- Basic design is done
- Ongoing simulations to create patterns, etc.
- Strip Card test Jan. '97

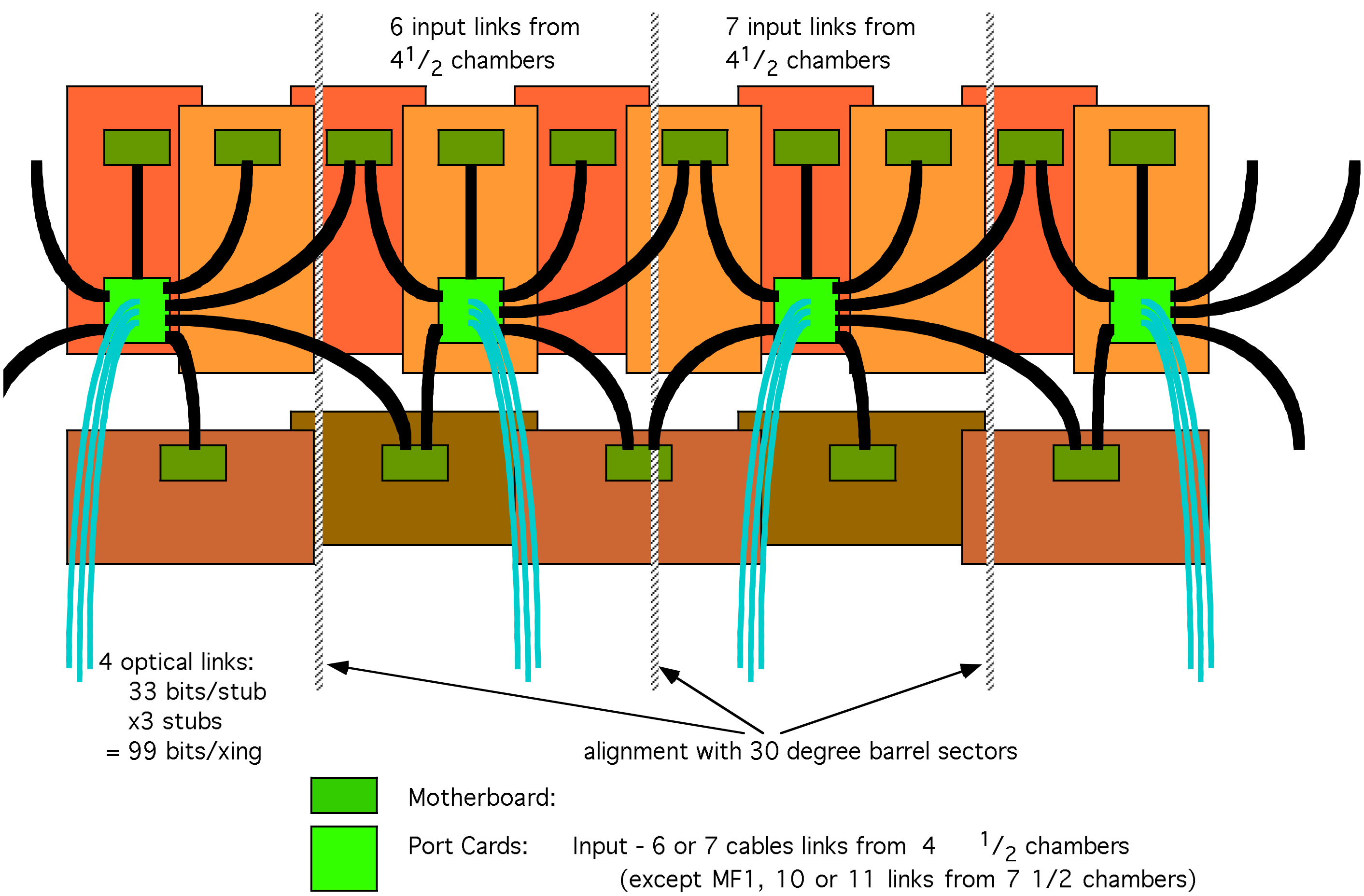
Revised CSC Trigger Layout



CSC Trigger Port Cards

- **Align data in 30 degree sectors**
  □
- **Resolve chamber ϕ overlaps**
  □
- **Reduce # of optical links**

Port Cards and CSC Trigger Wiring



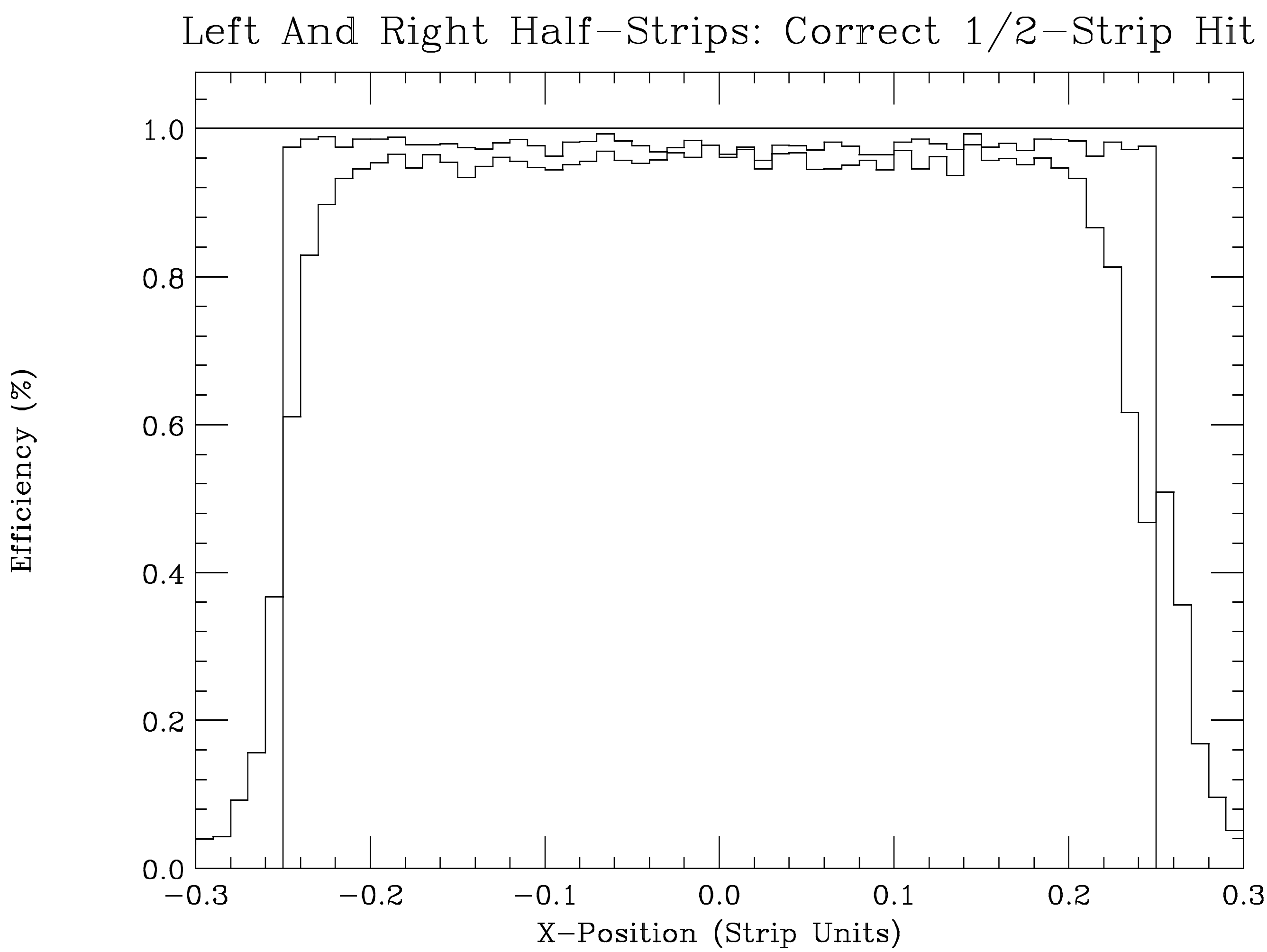
Discrete Comparators Test

P0 chamber prototype, CERN test beam

Korytov board

Gorn analysis

Eff(1/2-strip)=92%,   Eff(3/2-strip)=98%

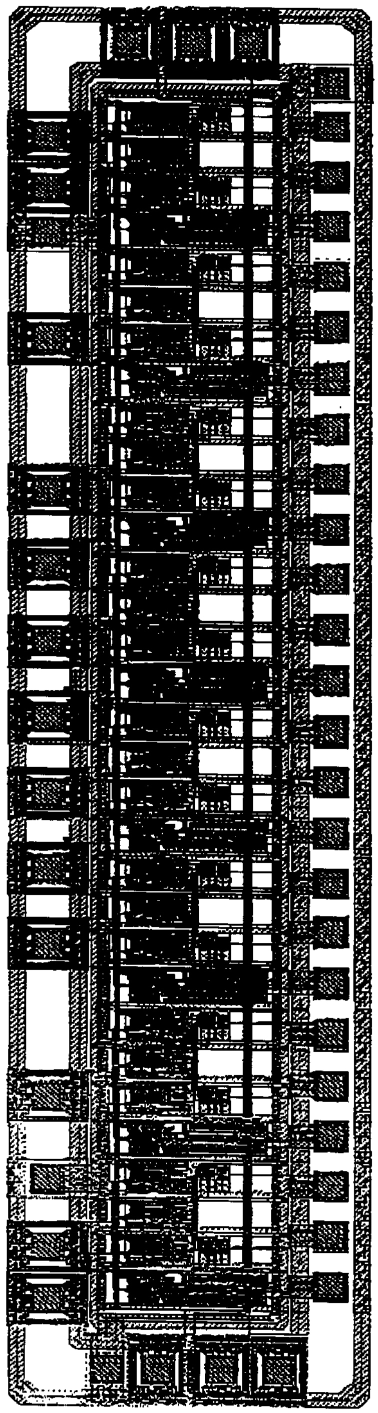


Comparator ASIC (Santiard)

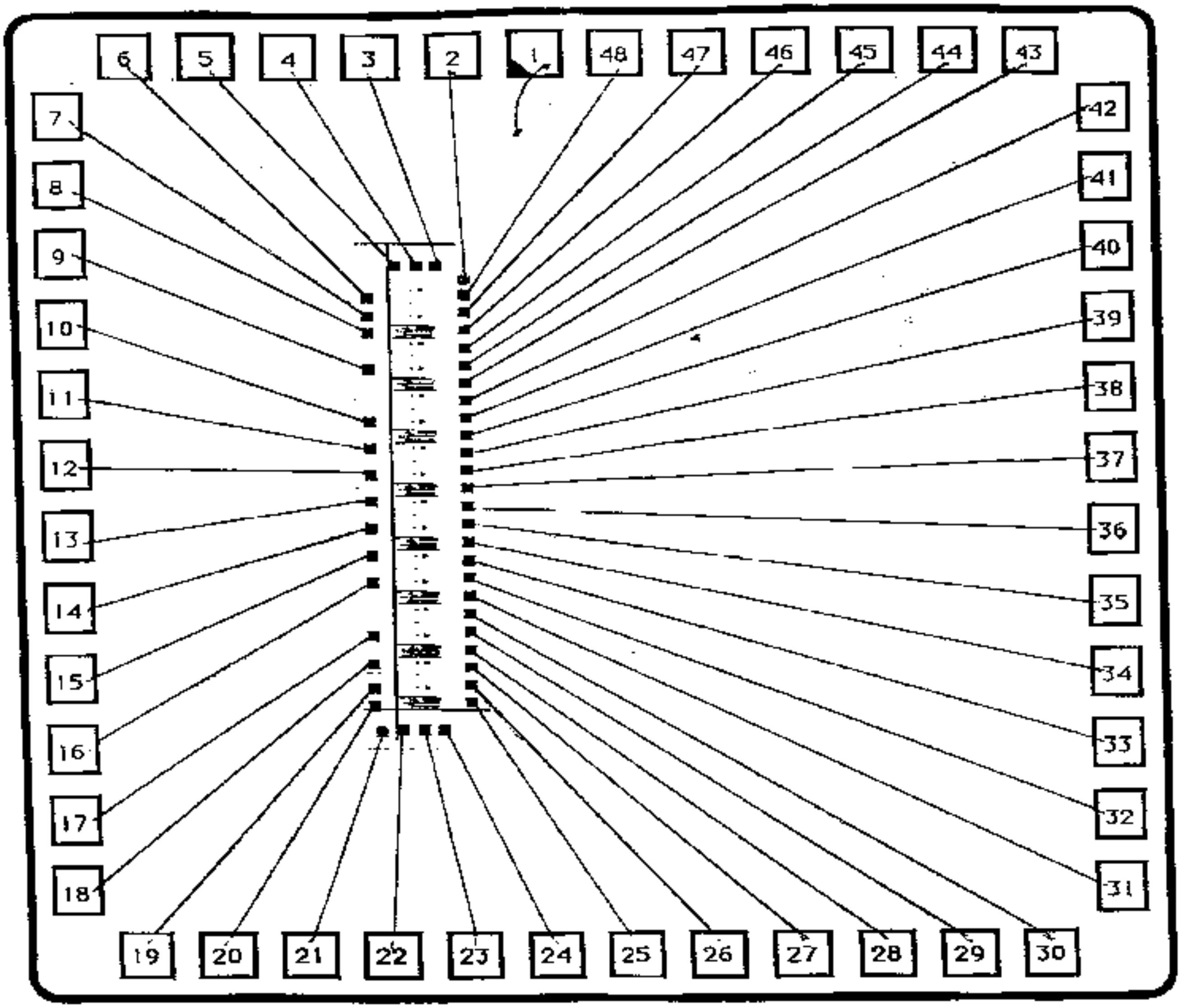
Santiard Strip Comparator ASIC

- Description in CERN-ECP/MIC, 16-04-96
  - Circuit design, simulation results
- Layout of 8-ch circuit is complete
- December delivery
  - Enough 8-channel chips to instrument P0 prototype plus spares
- Some modifications desired for 16-ch final version

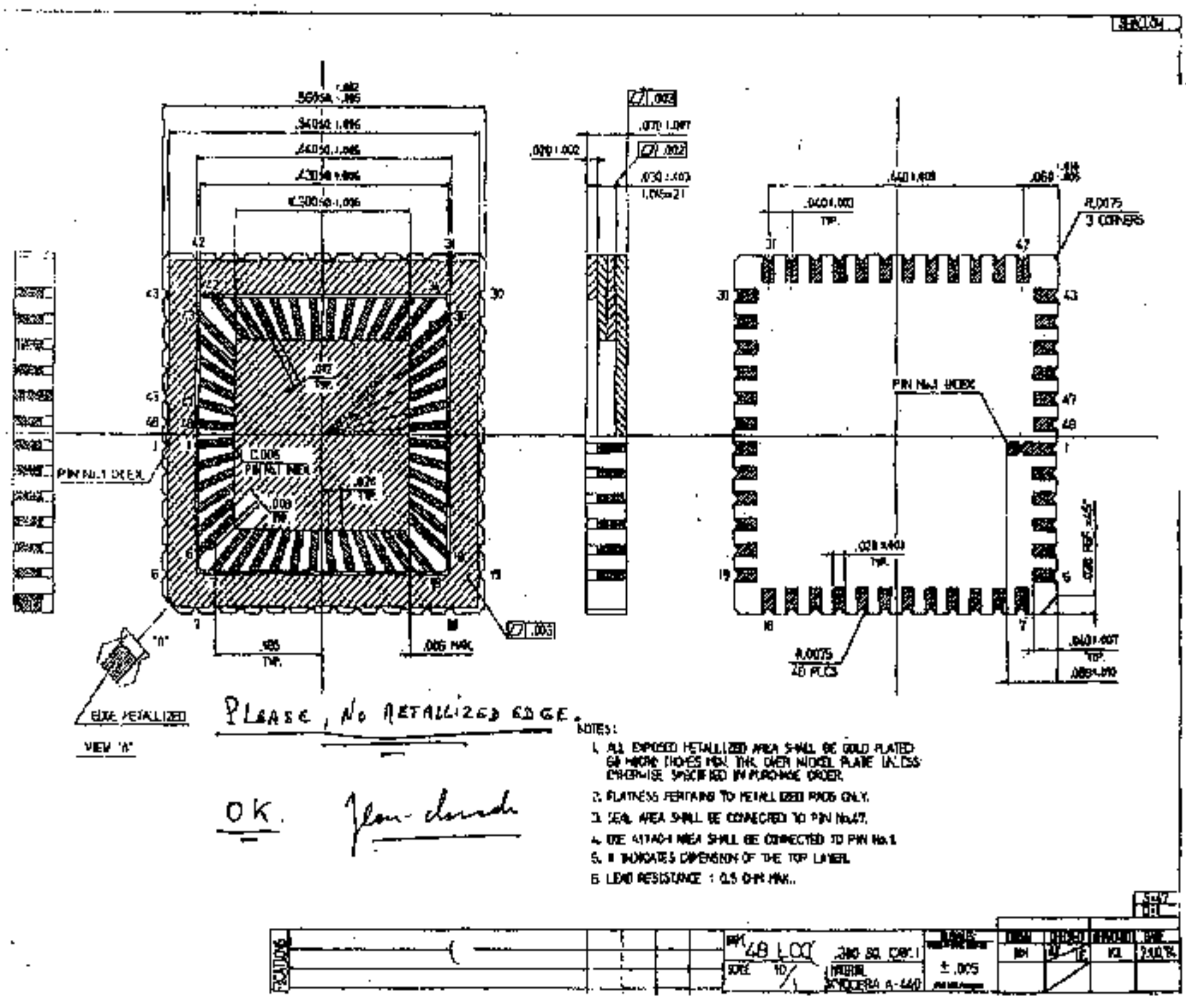
Comparator Layout



Comparator Package (internal)

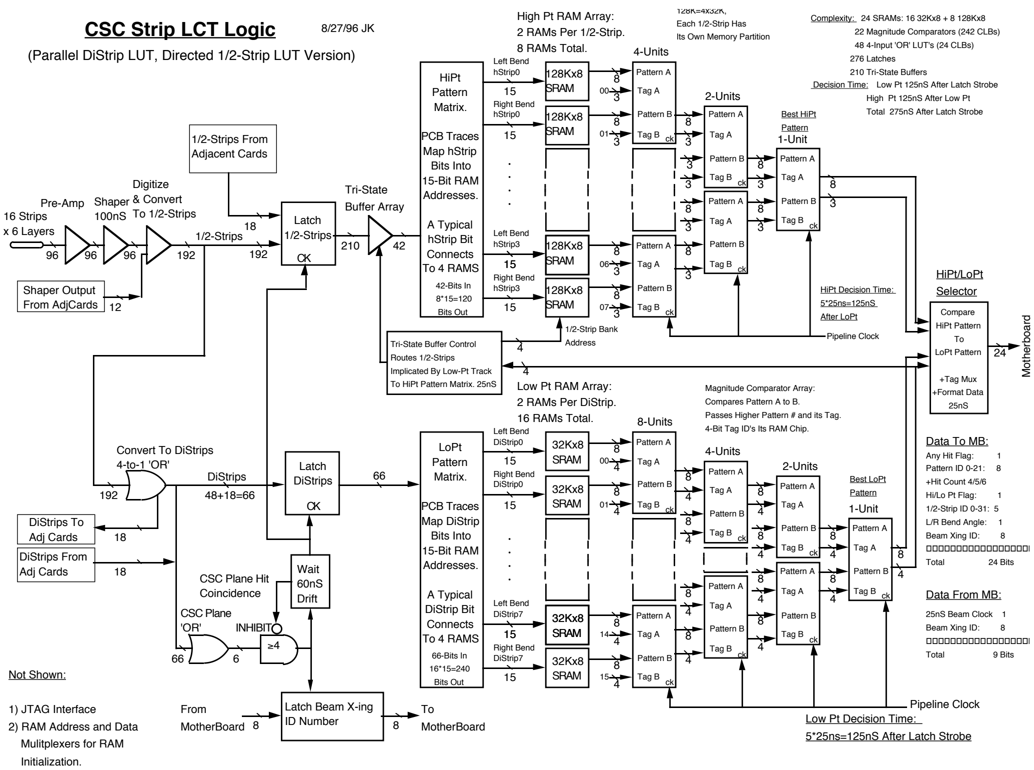


Comparator Package (external)



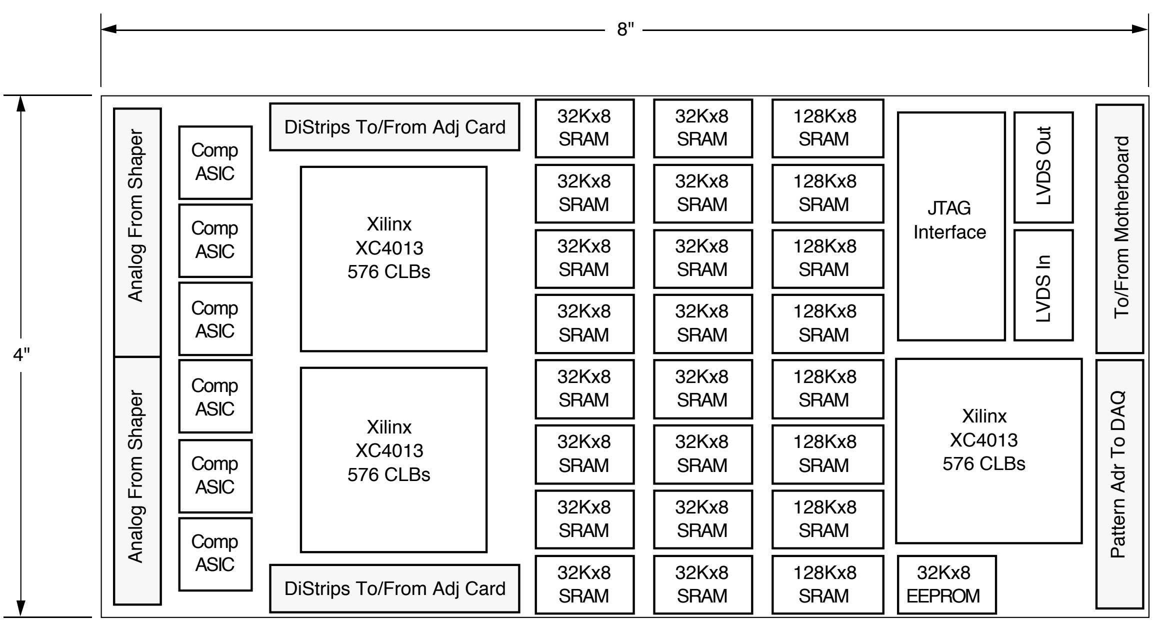
Trigger Logic and Board Layout

• J. Kubic



8/27/96 JK

Cathode Strip LCT Card



Prototype Test

Strip Trigger Card cosmic ray test

Feb. '97 with P0 chamber

Ohio State preamp/shaper ASICs

CERN comparator ASICs

UCLA pattern arrays and cards

UC Riverside readout