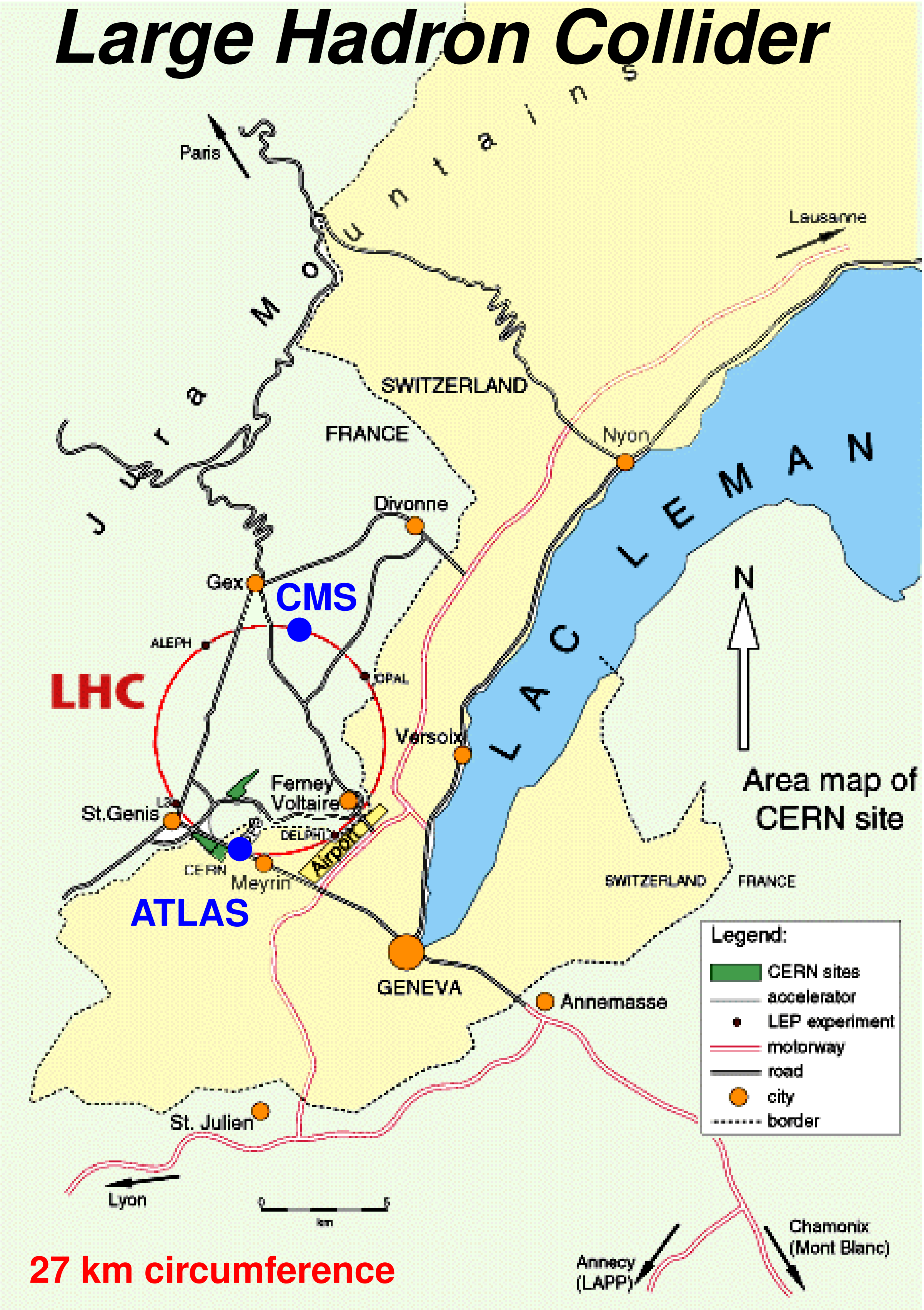
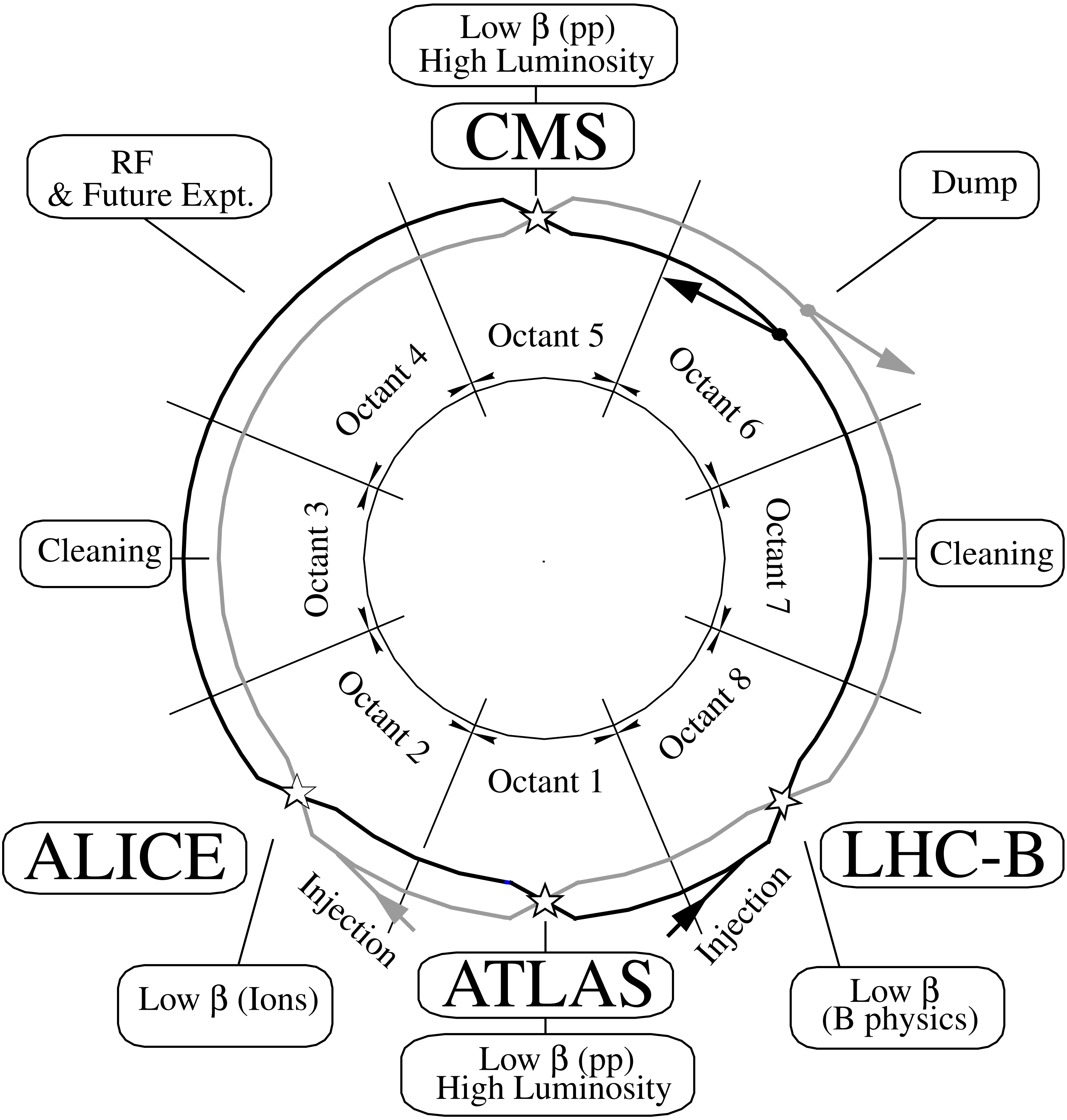
LHC & CMS

INTRODUCTION

Large Hadron Collider



Large Hadron Collider



Large Hadron Collider

Basic parameters

- **Collision energy:** **7+7 TeV**
- **Bunch crossing frequency:** **40 MHz**
- **Bunch spacing:** **25 ns $\Leftrightarrow$ 7.5 m**
- **Design luminosity:** **10^{34}cm^{-2}s^{-1}**
- **pp collisions per b.x.:** **~20**
- **Luminosity life time:** **~10 hours**

Useful numbers

1 LHC running year $\approx$ 1/3 calendar year $\approx$ 10^7s

- First 2-3 years: **"low luminosity"**
  10^{33}cm^{-2}s^{-1} = 10^4pb^{-1}/year = 10 fb^{-1}/year

- Later: **"high luminosity"**
  10^{34}cm^{-2}s^{-1} = 10^5pb^{-1}/year = 100 fb^{-1}/year

σ_{pp} (inelastic, without diffraction) **= 55 mb**

Rate [MHz] **=** σ [mb] $\cdot$ **L** [10^{33}cm^{-2}s^{-1}]

TRIGGER

and

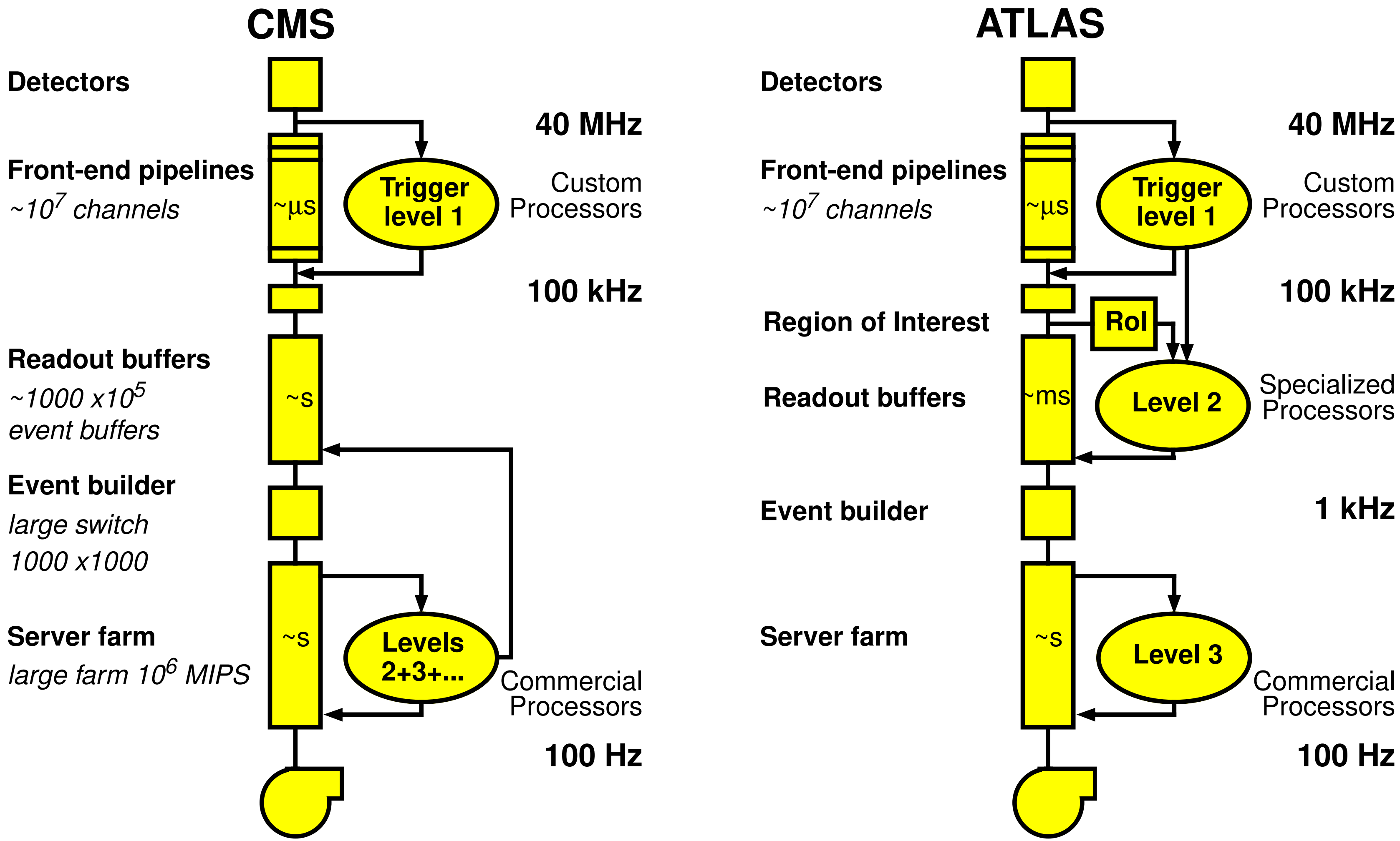
Data Acquisition

Data Volumes and Trigger Rates

detector	channels	occupancy	event size (kB)
Pixel	80 000 000	0.01 %	100
Inner Tracker	16 000 000	3 %	700
Preshower	512 000	10 %	50
Calorimeters	125 000	5 %	50
Muons	1 000 000	0.1 %	10
Trigger			10
CMS total	100 000 000		1 M Byte

level	criteria	input rate		process. time	method
first	bunch crossing	40 MHz	25 ns	~ μs	pipeline
higher	hard γ, e, μ, jets	100 kHz	10 μs	~ s	parallel
tape	b, W, Z	100 Hz	10 ms		parallel

Trigger Architectures



Pipeline processing

First level trigger has to analyse every bunch crossing (bx),
i.e. every 25 ns it has to decide to take given event or to drop it.

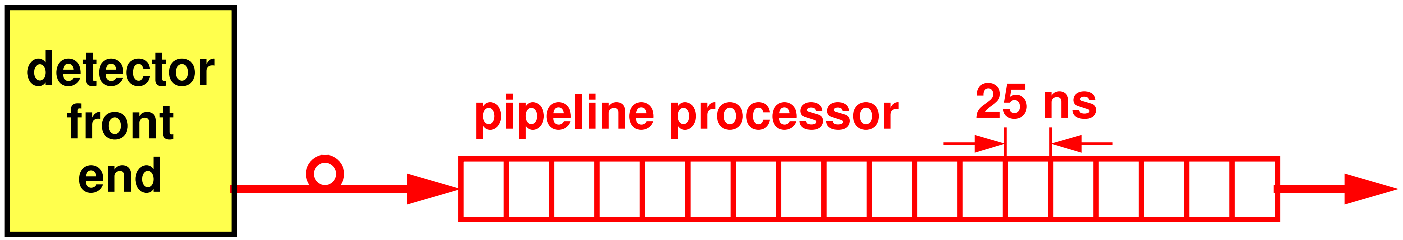
However, the decision takes much longer.
Solution: pipeline processing.

Trigger algorithms are divided in 25 ns steps.
Trigger processor is a chain of cells,
each one performing one algorithm step.

Given cell at the end of each 25 ns steps sends its results to the next cell
and it is ready to receive results form the previous cell.

Thus, the trigger data “drift” through the pipeline, being processed.

They arrive to the end of the chain in a form of YES/NO answer,
every 25 ns, with fixed delay wrt physical event.



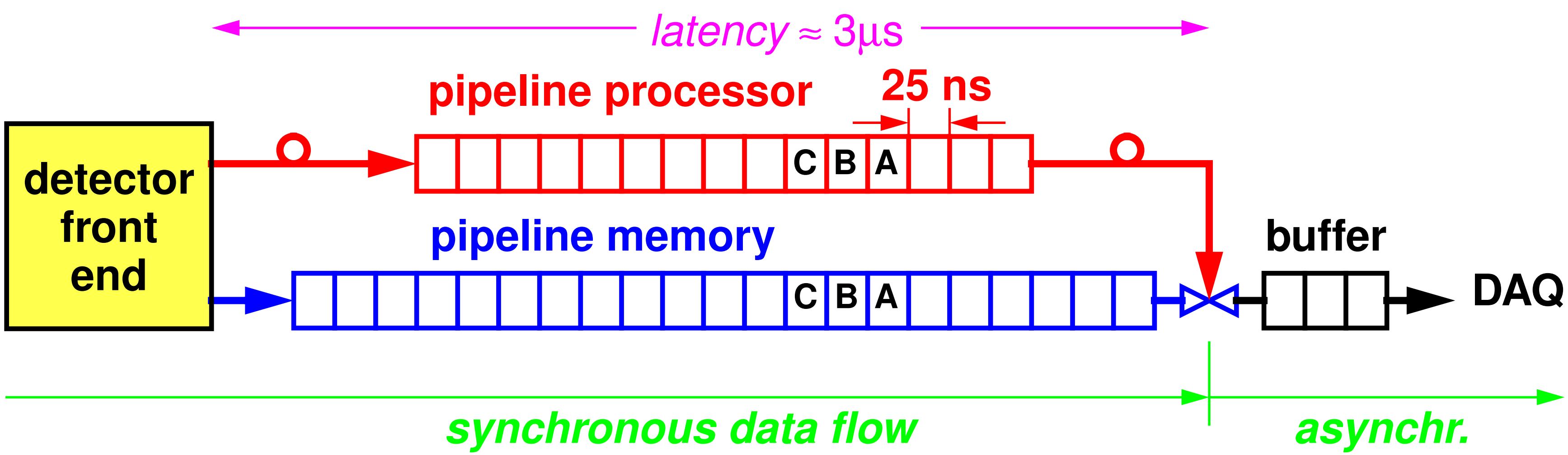
Pipeline memory

Data must wait for the trigger decision in <u>pipeline memory</u>
i.e. shift register, driven by 40 MHz (25 ns) clock.

Analogue pipeline memories (needed for tracker) **are limited to ~130 steps.**
This limits the first level trigger latency to ~3μs.

<u>Trigger latency</u> =

- **trigger data transfer time** *(optical links to the control room)* **+**
- **trigger processing time +**
- **trigger decision distribution time** *(optical links back to the detector)*



FIRST LEVEL

MUON

TRIGGER

Resistive
Plate
Chambers
in CMS

Muon Trigger Detector

Ideal muon trigger detector should have the following features:

- **excellent time resolution:** σ **~ 2 ns**
  - to recognize bunch crossing
- **good resolution in Rϕ coordinate:** **~ 1 cm**
  - to measure bending in the magnetic field
- **moderate resolution in RZ coordinates** **~ 1 m**
  - because $p_t(\Delta\phi)$ relation depends on Z
  - to be able to see several muons in one event

Scintillator or silicon strips would be too expensive.

CMS has chosen Resistive Plate Chambers.

RPC System in CMS

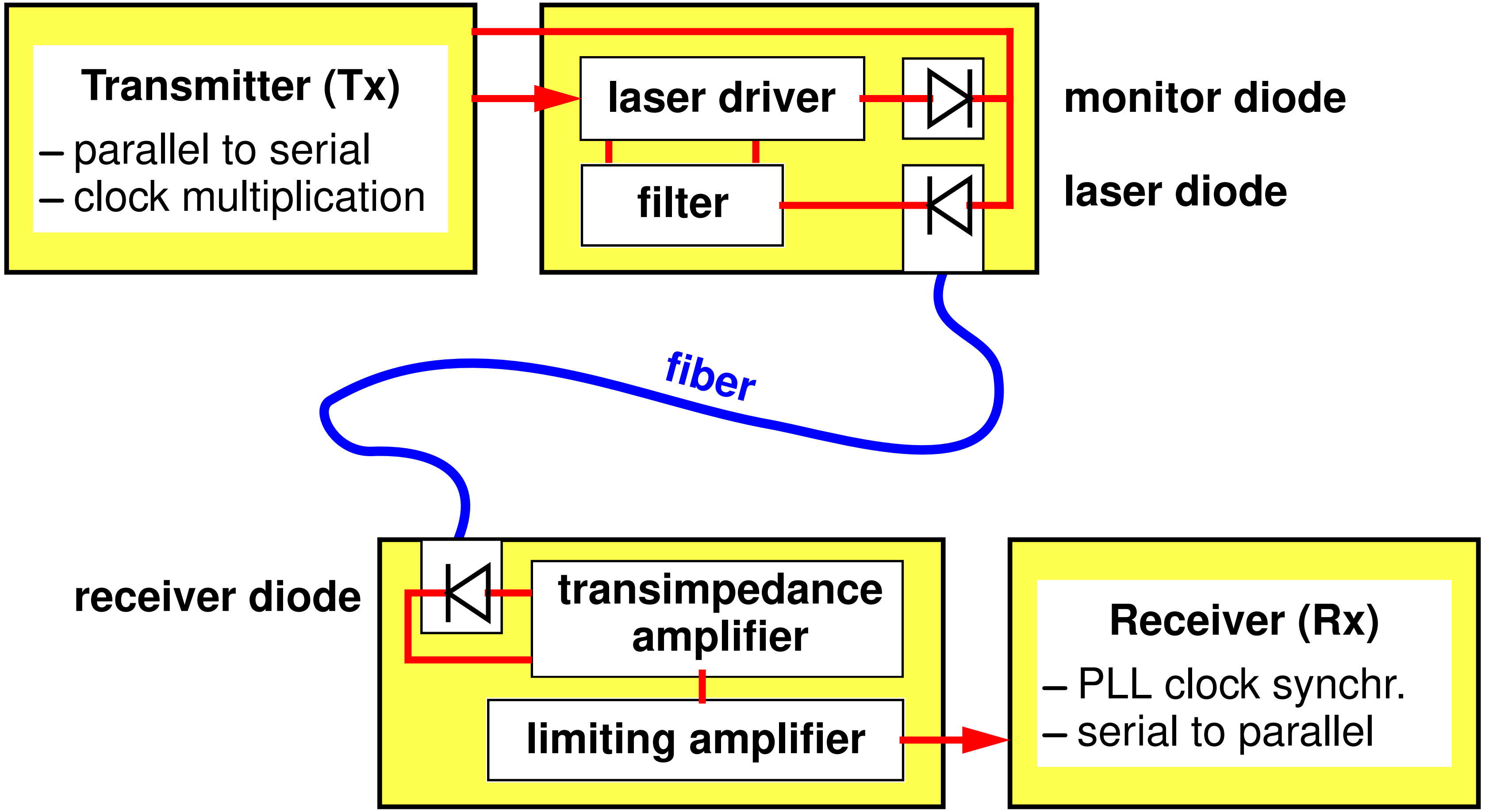
	baseline ($\|\eta\|<2.1$)		**upgrade** ($\|\eta\|<2.4$)
	barrel	**endcap**	
area	**2100 m^2**	**1100 m^2**	**+ 60 m^2**
chambers	**780**	**648**	**—**
channels	**75 000**	**90 000**	**+ 28 000**

The numbers are only approximate because the mechanical design is not yet finalised.

OPTICAL LINKS

in CMS

Optical Link Elements



CMS Data Link Test Board

Possible start-up for Korean participation in CMS

Possible start-up for Korean Groups

- **Work on Link Test Setup at CERN**
  – to gain experience with the hardware
- **Copy the Link Test Board + Tx / Rx Daughter Board**
  – to use it at home
- **Develop new Tx / Rx Daughter Boards for other chipsets**
  – perhaps made in Korea
- **Study various link protocols and data compression algorithms**
  – e.g. RPC data compression

Pattern Comparator Trigger

PACT

PACT Segmentation

hardware	logical unit	subdivision	$\Delta\phi$	$\Delta\eta$	quantity	
channel	strip	—	5/16°	0.1-0.2	164 736	27 648
PAC	segment	8 strips/ref.pl.	2.5°	0.1-0.2	4752	864
TR Board	sector	12 segments	30°	0.1-0.2	396	72
TR Crate	ring	12 sectors	360°	0.1-0.2	33	6
Rack	super-ring	3 rings	360°	~0.35	11	2

PAC = Pattern Comparator ASIC

ref.pl. = reference plane

TR = Trigger and Readout

Quantity is given for the baseline ($|\eta|<2.1$)
and for the upgrade ($2.1<|\eta|<2.5$)

Synchronisation Unit (SU)

Signals coming from different muon stations have to be corrected for:

- **particle time of flight**
- **RPC response time**
- **signal propagation along the wire**
- **cable length**

Before they enter the trigger coincidence they have to be

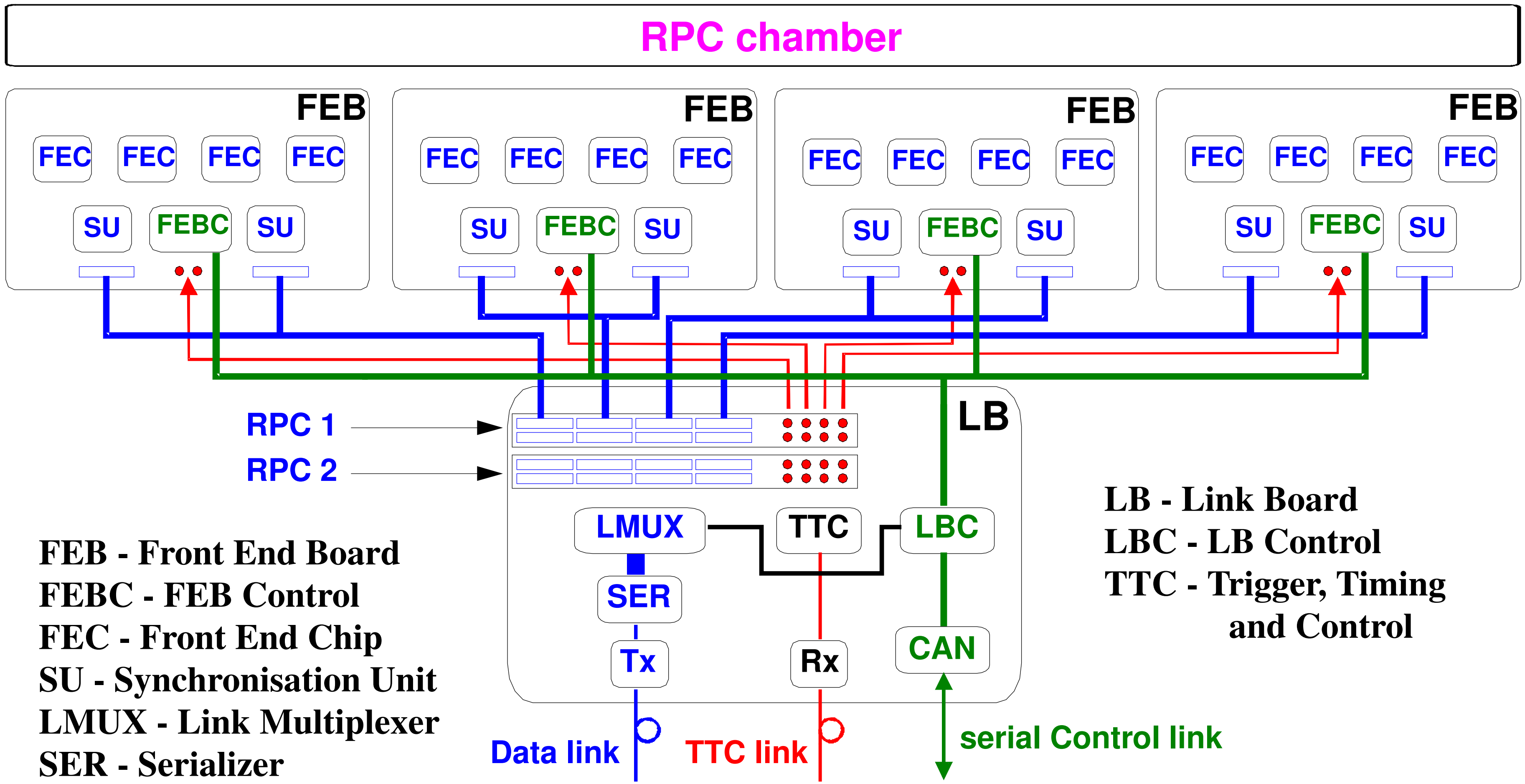
- **shaped to a given length**
- **aligned with the LHC clock distributed by the TTC system**

These functions are performed by Synchronisation Unit.

Pulse length and delay can be programmed

- **with the precision of ~1 ns**
- **for each group of 6 or 12 channels independently**

RPC Front-End



1 LB = 2-3 RPC 1 RPC = 4 FEB = 16 FEC = 96 strips 1 FEC = 6 strips

Front End Board Controller (FEBC)

Tasks:

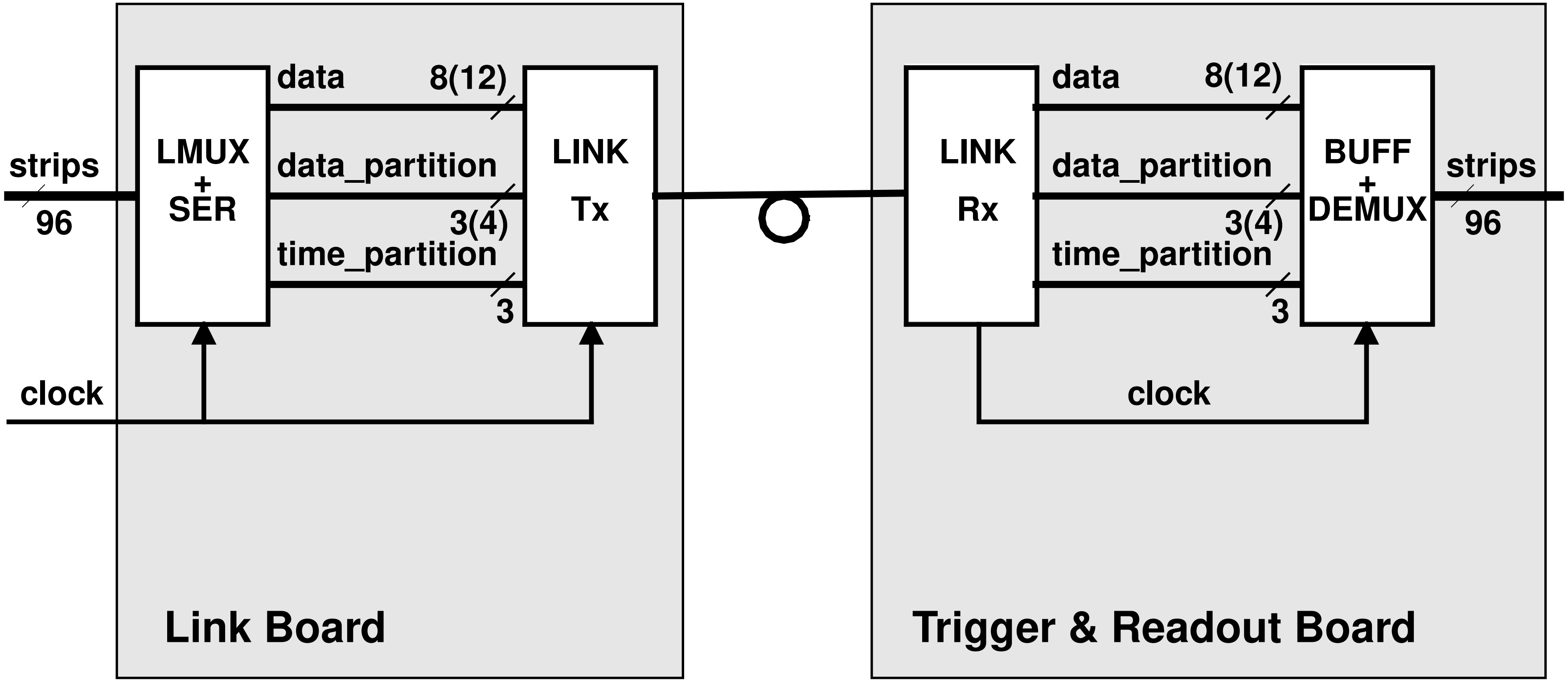
- **store and distribute the FEC thresholds,**
- **set the test pattern and test sequence and furnish them in a precise, synchronous way to test input of FECs,**
- **set the time window properties for the SU ASICs,**
- **read out the SUs test histograms.**

Control of the FEBC is provided via FEBC bus from the Link Board.

The discriminator thresholds and test bit patterns must be set before enabling the data acquisition.

The sequence of tests with one or several test bit patterns can be started with broadcasted test pulse signal after the data acquisition has been enabled.

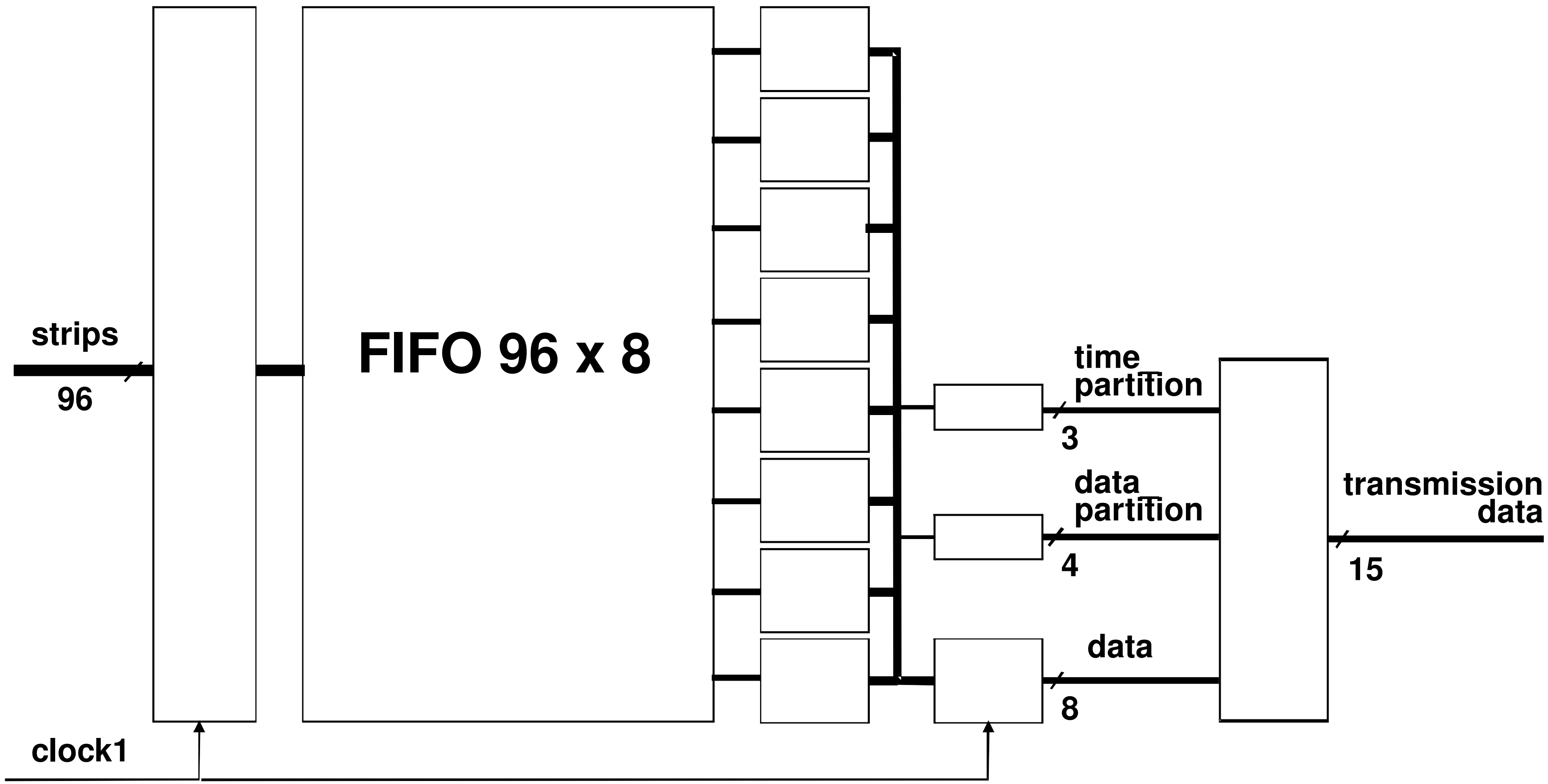
RPC data transfer



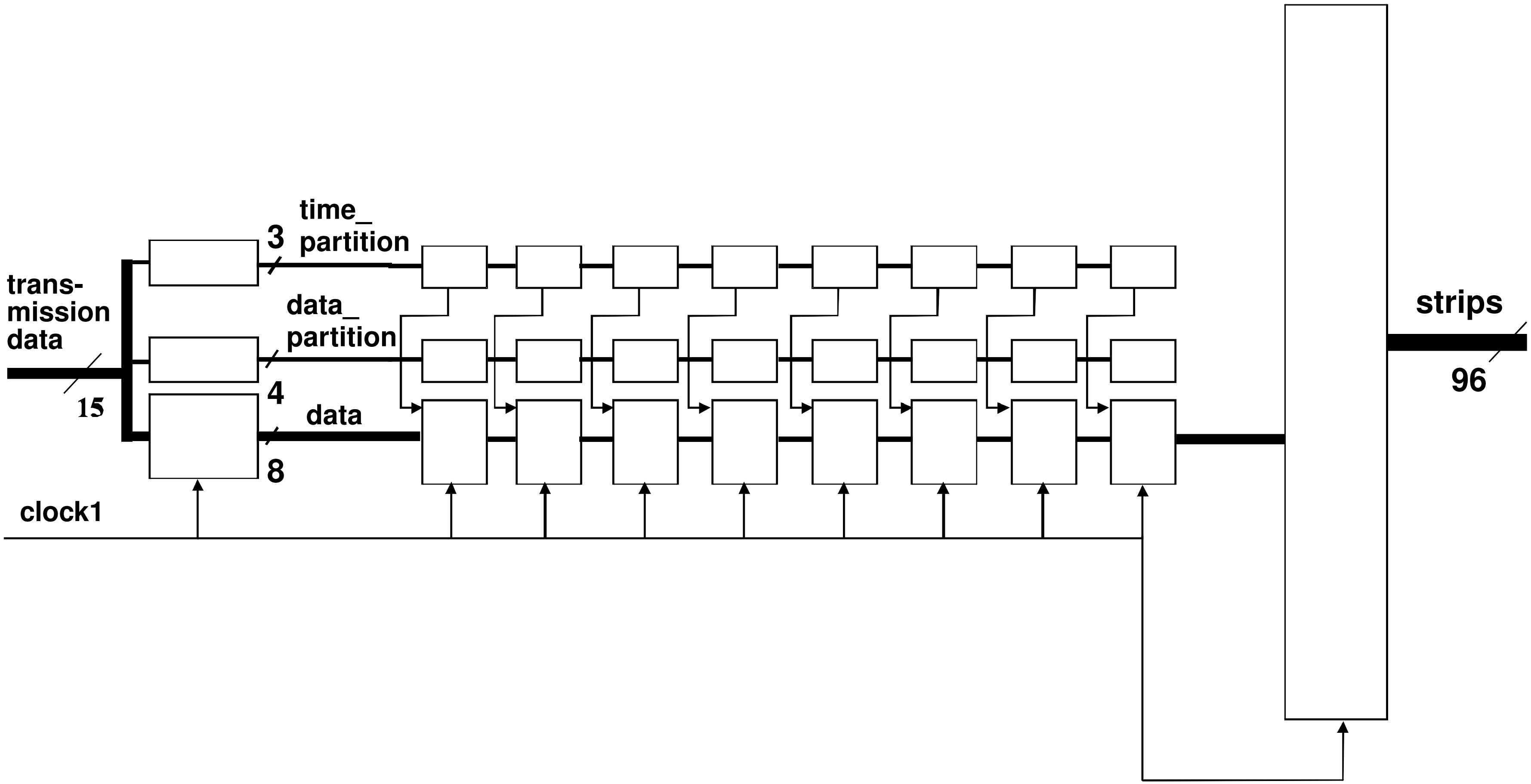
on the detector

in the trigger room

RPC data transmission: LMUX

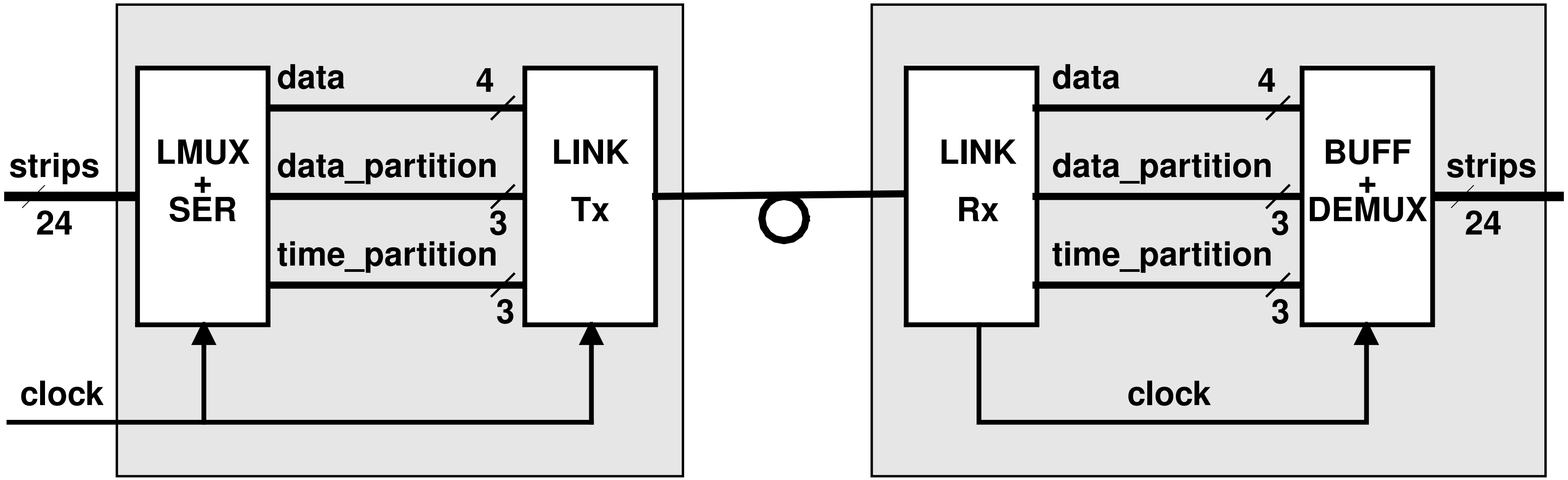


RPC data transmission: DEMUX



RPC data transmission: FPGA model

Limited version: 1/3 size, 1/2 speed



Altera EPF81500GC280	**Altera EPF8820AGC192**
pins: 35 / 204	**pins: 38 / 148**
cells: 1130 / 1296 (87%)	**cells: 272 / 672 (40%)**

LMUX / DEMUX FPGA model

Idea of data compression/decompression (LMUX/DEMUX) works:

- **latency of data coding/decoding for gate array implementation should not exceed 2+ buffer_length + 2 = 12 (16),**
- **LMUX is more complicated,**
- **DEMUX can incorporate additional functionality**
  - η-data merging, synchronisation.

Gate array implementation necessary,
but first some questions should be answered:

- **what are the link parameters?**
  - frequency, multiplexing/demultiplexing factor
- **more study needed to decide the form of data partitioning:**
  - how long buffer_length should be?
  - how many data partition are needed?
- **data quality monitor should be implemented.**
- **DEMUX should be supplemented with synchronisation and data merging parts.**

Trigger and Readout Board (TRB)

Data received via optical fibers connected at the back of the crate.

Two options are being envisaged:

- **TRB as a single board**
- **two boards: Trigger Board and Readout Board connected to opposite sides of the custom backplane**
  – like the Calorimeter Regional Trigger Crate

Provision for tracks crossing TRB boundaries:

- **data to η-neighbours are sent via passive optical splitters before TRB**
- **data to ϕ-neighbours are sent via the backplane**

System layout:

- **13 racks,   39 crates,   39 x 12 = 468 TRB**