International Workshop on LHC-CMS Taejon, 24-26.02.97

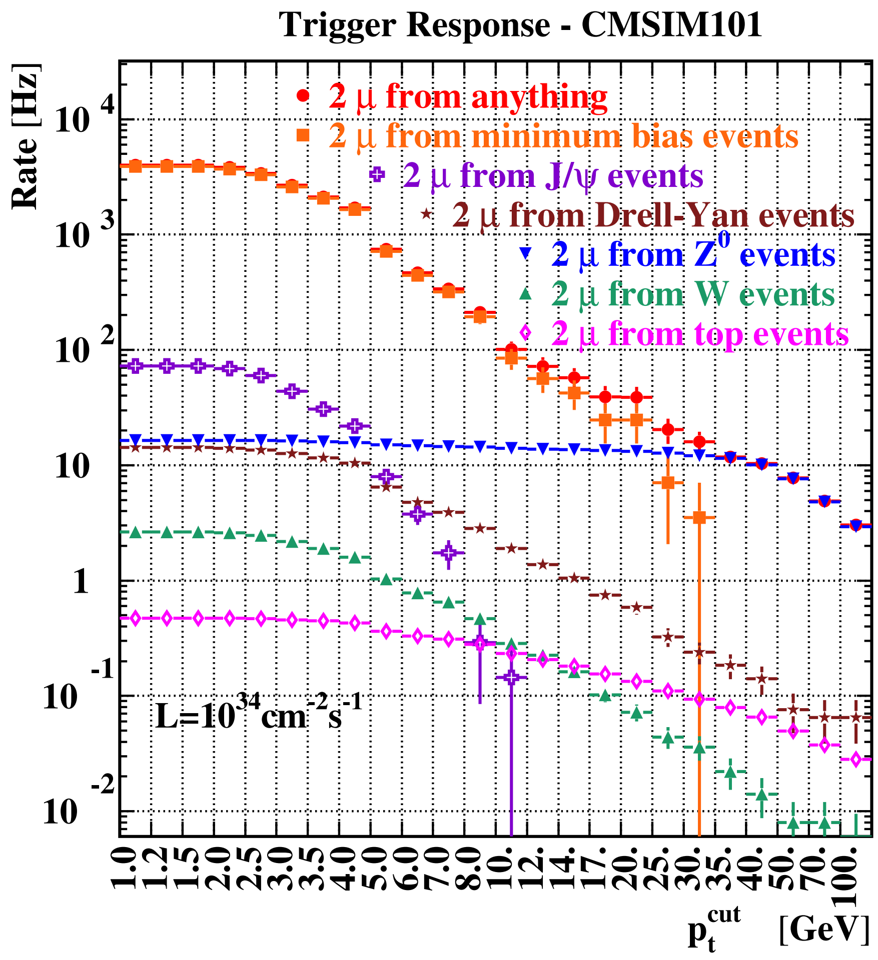
Muon Trigger

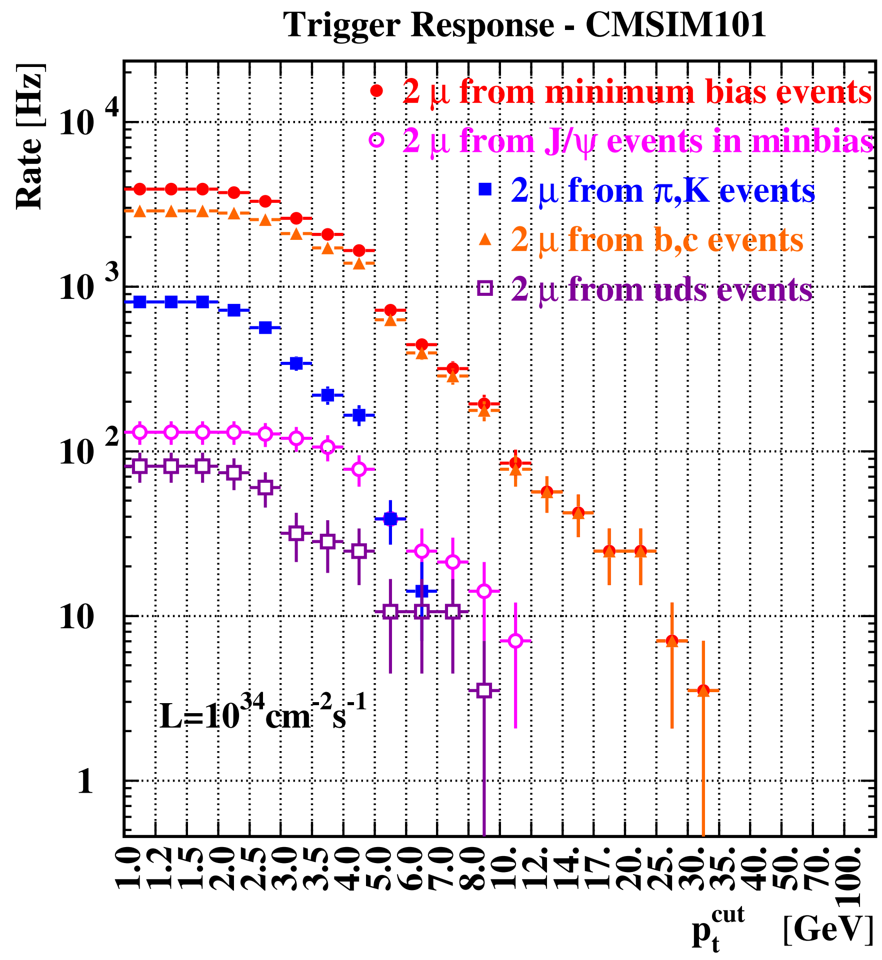
Grzegorz Wrochna
CERN

wrochna@cern.ch

- **CMS Muon Trigger System**

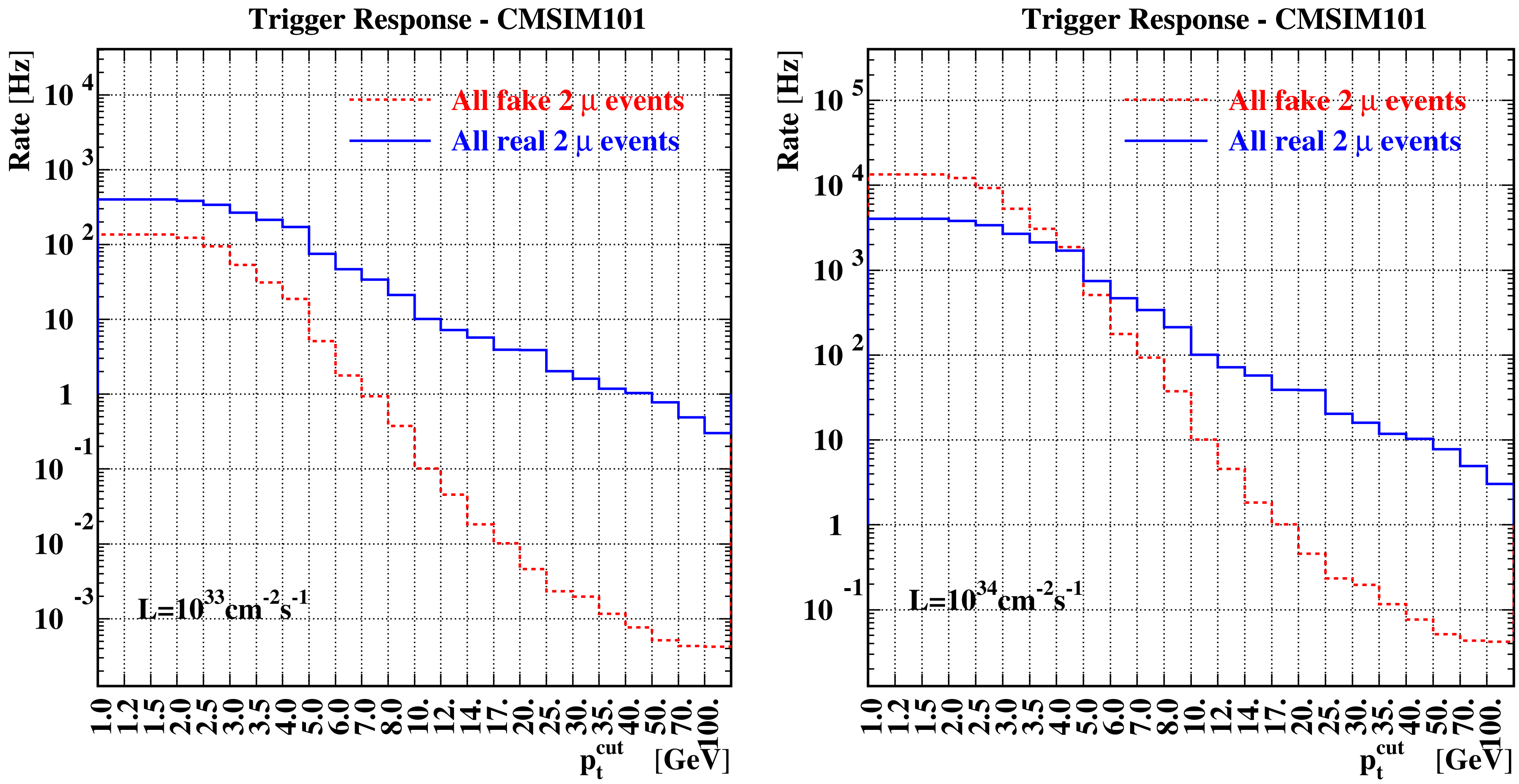
2-muon trigger rates





A. Fengler

Real & fake 2-muon trigger rates



Fake trigger: pileup of 2 muons from 2 different pp collisions

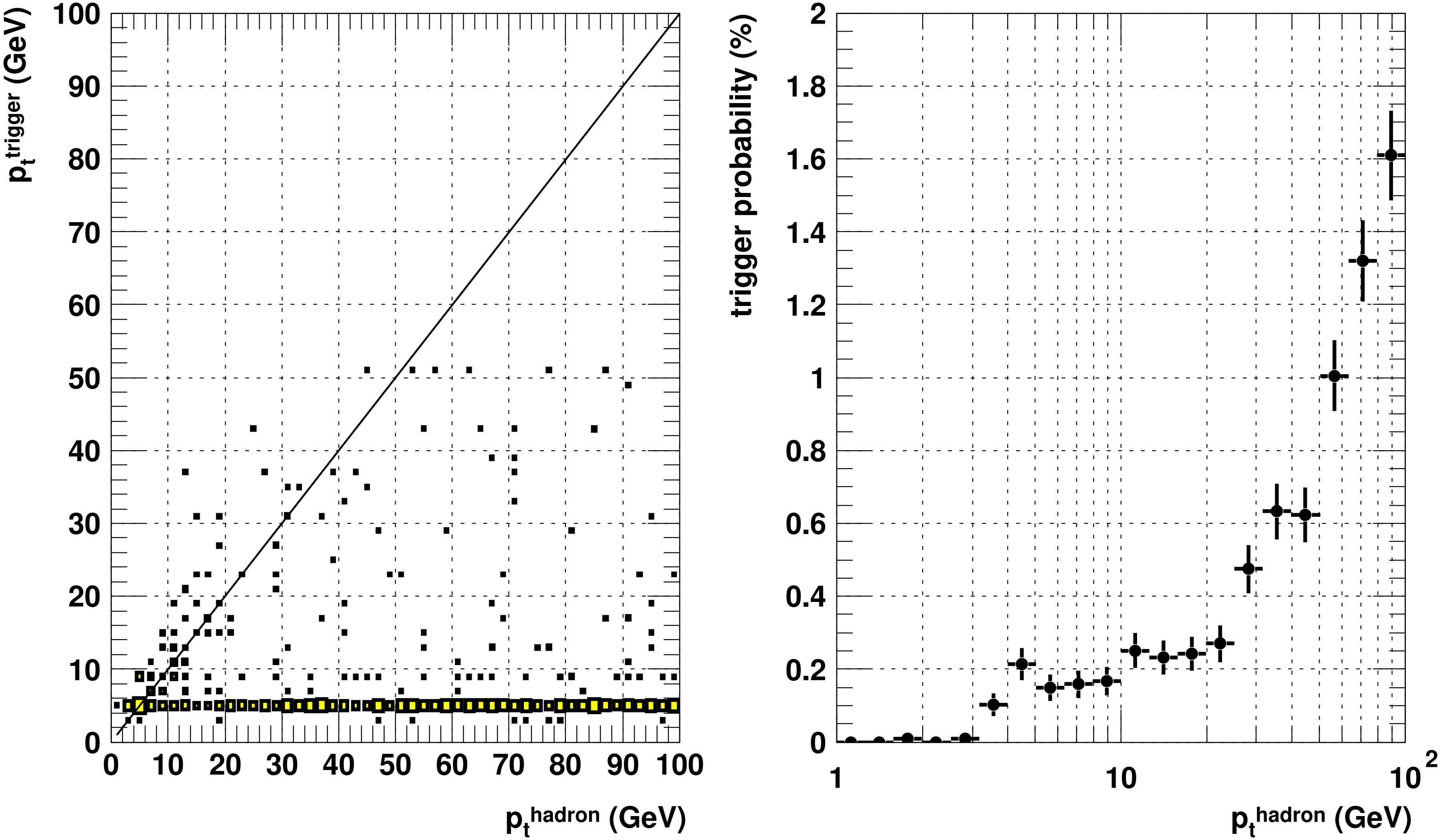
A. Fengler

Muon and Calorimeter Trigger Rates

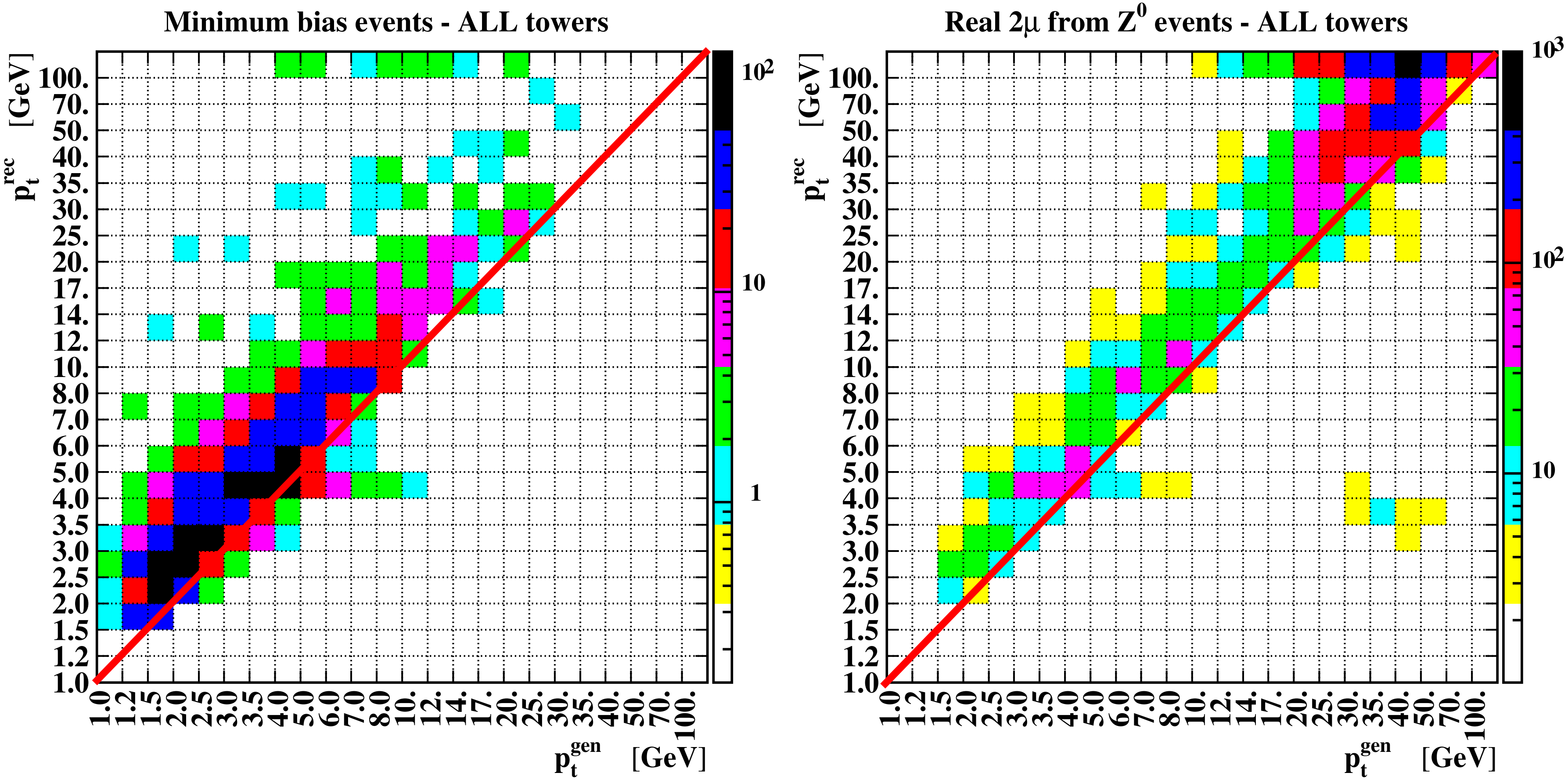
	$L = 10^{33}cm^{-2}s^{-1}$			$L = 10^{34}cm^{-2}s^{-1}$		
trigger type	threshold [GeV]	rate [kHz]	cumulative rate [kHz]	threshold [GeV]	rate [kHz]	cumulative rate [kHz]
μ	7	9.8	9.5	20	7.8	7.8
$\mu\ \mu$	2-4	0.5	10.1	4	1.6	9.2
μ e/γ	2-4, 6	2.5	12.2	4, 8	5.5	14.4
$\mu\ e_b$	2-4, 5	3.5	13.4	—	—	—
μ j	2-4, 12	2.2	14.5	4, 40	0.3	14.4
$\mu\ E_t^{miss}$	2-4, 40	0.8	14.7	4, 60	1.0	15.3
$\mu\ \Sigma E_t$	2-4, 150	0.8	14.7	4, 250	0.2	15.3

threshold = 2-4 GeV means: 4 GeV in the barrel, 2 GeV in the endcaps

Hadrons causing muon trigger



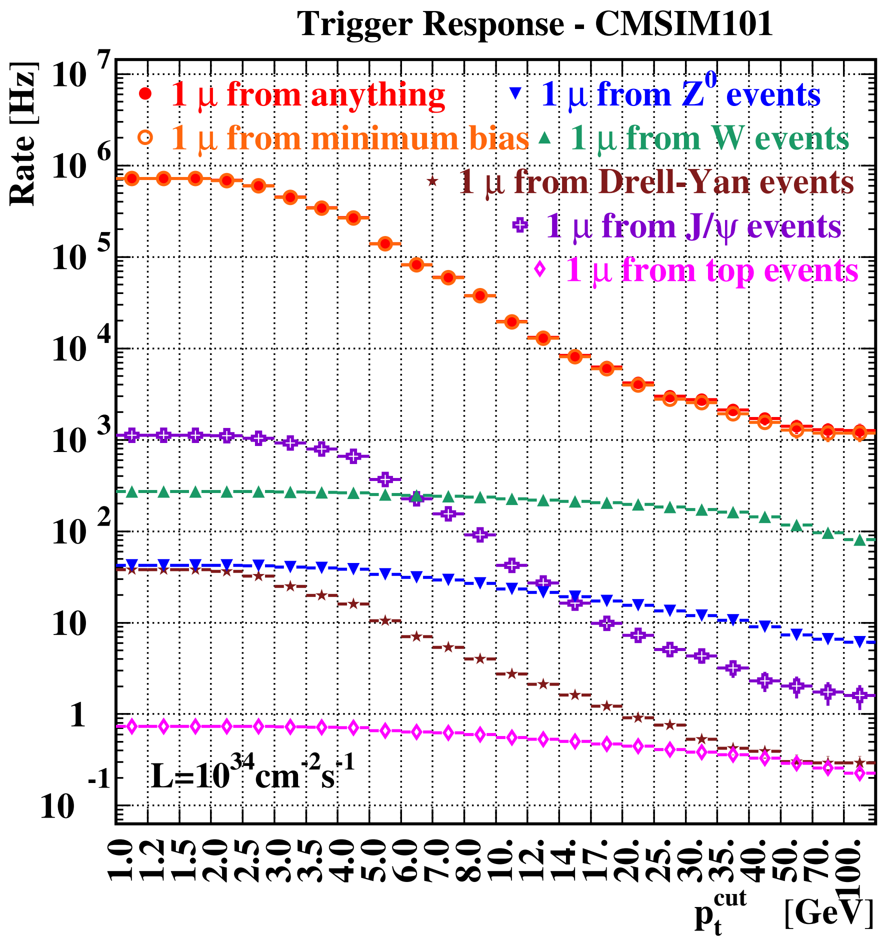
Trigger answer vs real muon p_t

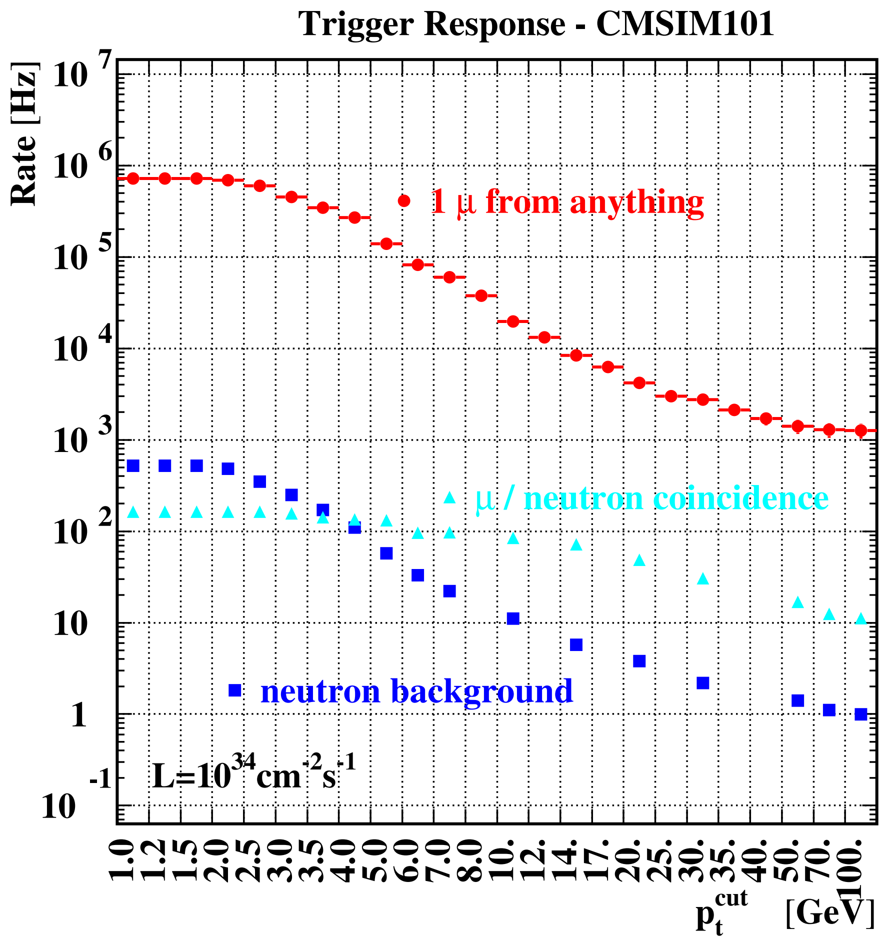


Trigger should never underestimate muon momentum

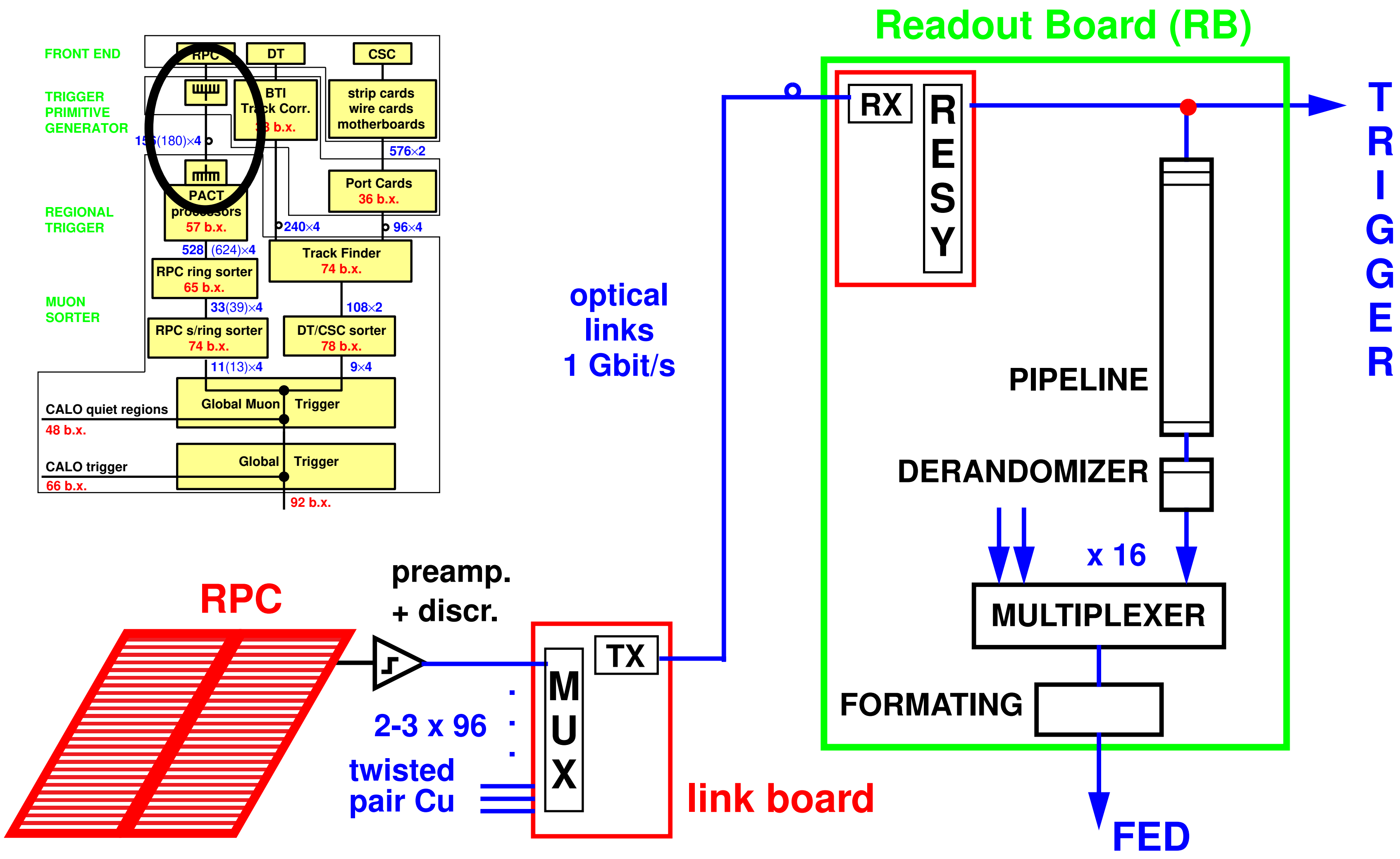
A. Fengler

Single muon trigger rates





RPC Readout System



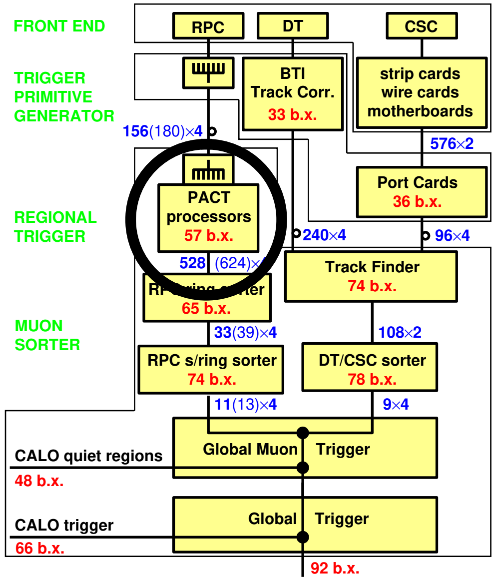
STATUS

of the Muon Trigger Project

PERFORMANCE

of the Muon Trigger System

RPC PAttern Comparator Trigger



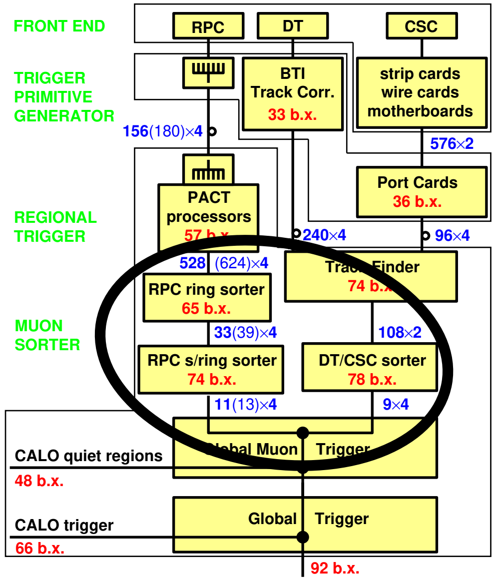
STATUS: DONE

Milestone D300 — November 96

Review of test benches with FPGA prototypes of PAC and synchro/readout chips ***(Warsaw)***

The test bench of the Pattern Comparator Trigger for RPC will consist of 4 cards: synchronisation, trigger, readout, and control. They will be equipped with FPGA versions of the Pattern Comparator (PAC) chip and the synchronisation module. The RD6 ROC ASIC will be used for the readout. The primary purpose is to test the system aspects of the complete muon trigger setup. The setup will be equipped with boundary scan, which will be used for testing and programming. The modular structure of the test bench will allow for changes from FPGA's to ASIC's once the latter are available (D350).

Muon Sorter



Milestone D310 — November 96

Review of FPGA prototype tests of the muon sorter ASIC (Bari)

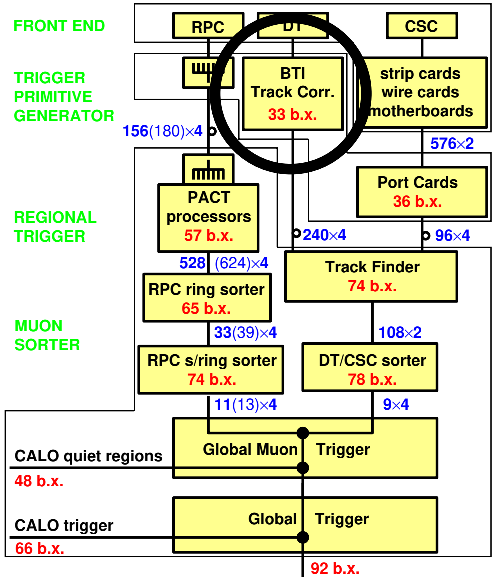
The muon sorter selects 4 highest momentum muons in the entire muon trigger system. It is a tree-like structure of sorter chips, each one selecting 4 out of 8 muons. FPGA versions of this chip will be tested in the test bench (D300).

STATUS:

DONE

The test bench has been build and equipped with the PAC and SORTER prototypes. It has been successfully tested in lab in Warsaw, summer 96. In autumn 96 it was connected to the RPC cosmic telescope in Bari and tested with cosmic muons.

Drift Tube Trigger



Milestone D320 — November 96

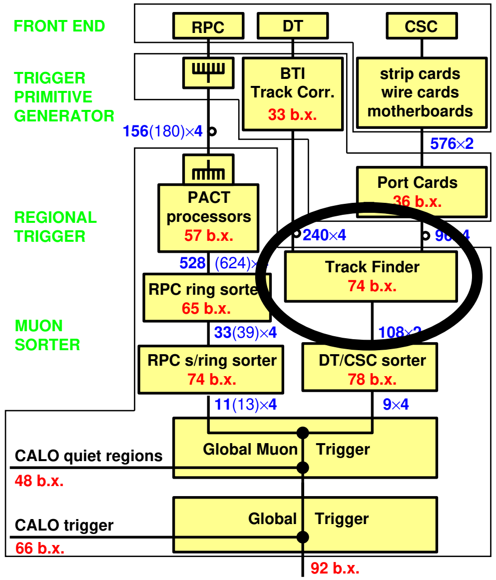
Review of FPGA prototype tests of the meantimer ASIC (Padova)

Three meantimer prototypes in a FPGA reduced version, mounted on a 6U VME card, have been tested on H2 beam in summer '95. Detailed analysis of their performance will be completed.

STATUS: DONE

The tests of the chip (now called *Bunch and Track Identifier BTI*) have been completed in spring 96. The results have been used as an input to simulate the full size chip.

DT/CSC Track Finder



Milestone D330 — March 97

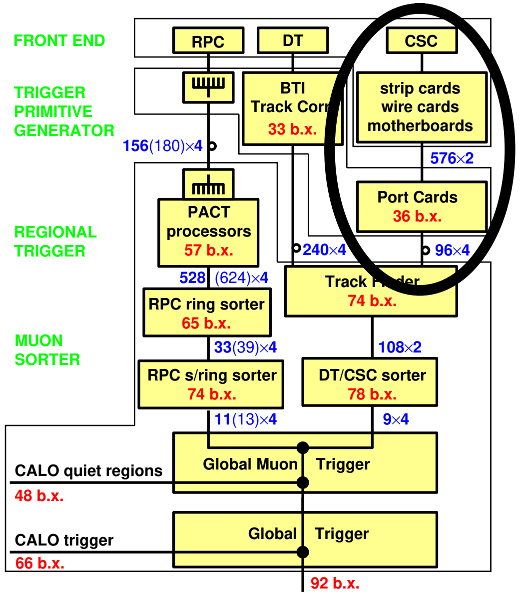
[Review of FPGA prototype tests of the Track Finder ASIC's] *(Vienna)*

The hardware implementation of the track finder is going to be tested using a FPGA prototype system. In the first testing phase the chamber electronics will not be available, thus the track finder prototype will be evaluated in a prototype test bench. This test bench will deliver simulated physics data to the FGPA prototype.

STATUS: in progress

All FPGA's and boards of the test bench have been designed in summer 96. The FPGA's are already programmed and the boards are now being manufactured and assembled.

CSC Trigger



STATUS:

in progress

Milestone D340 — February 97

Delivery of prototypes of comparator tree chips for cathode strip chamber trigger (UCLA, Florida, CERN)

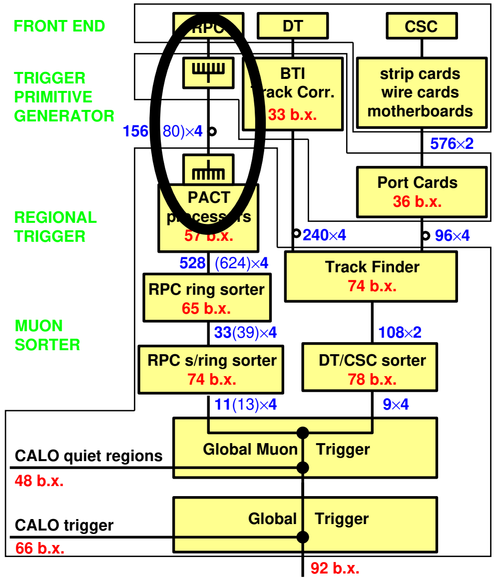
The CSC chamber strip preamp/fast shaper ASICs plus strip comparator tree ASICs will be connected to 16 strip x 6 layers of a CSC prototype chamber and tested for efficiency and spatial resolution.

Milestone D342 — April 97

Delivery of prototypes of pattern finding chips for cathode strip chamber trigger (UCLA, Florida, CERN)

The CSC chamber strip pattern-finding FPGAs will be connected to 16 strip x 6 layers of a CSC prototype chamber and tested for efficiency and spatial resolution.

RPC Readout System



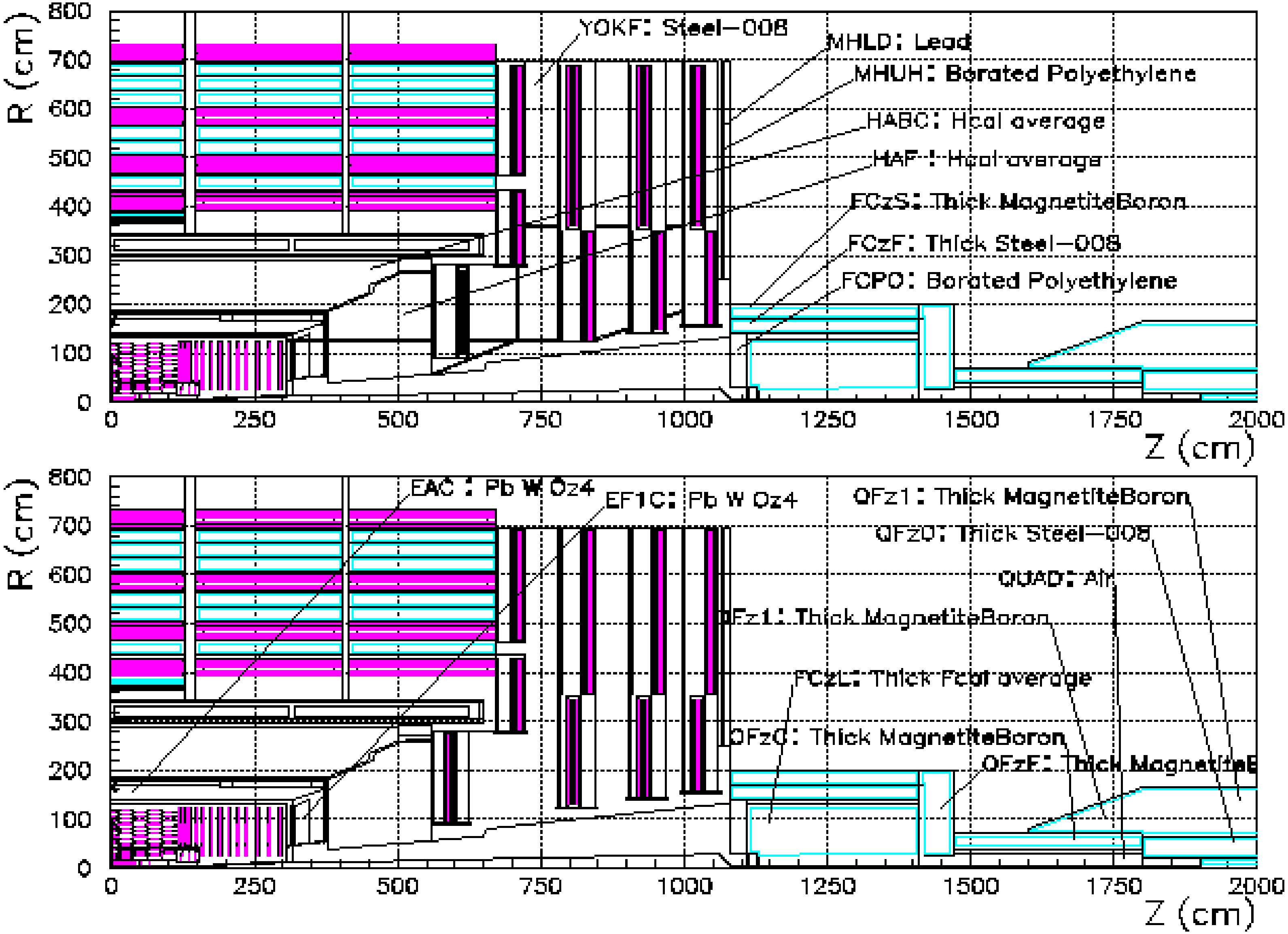
STATUS:
awaiting

Not covered yet

Korean Groups are heartily welcome

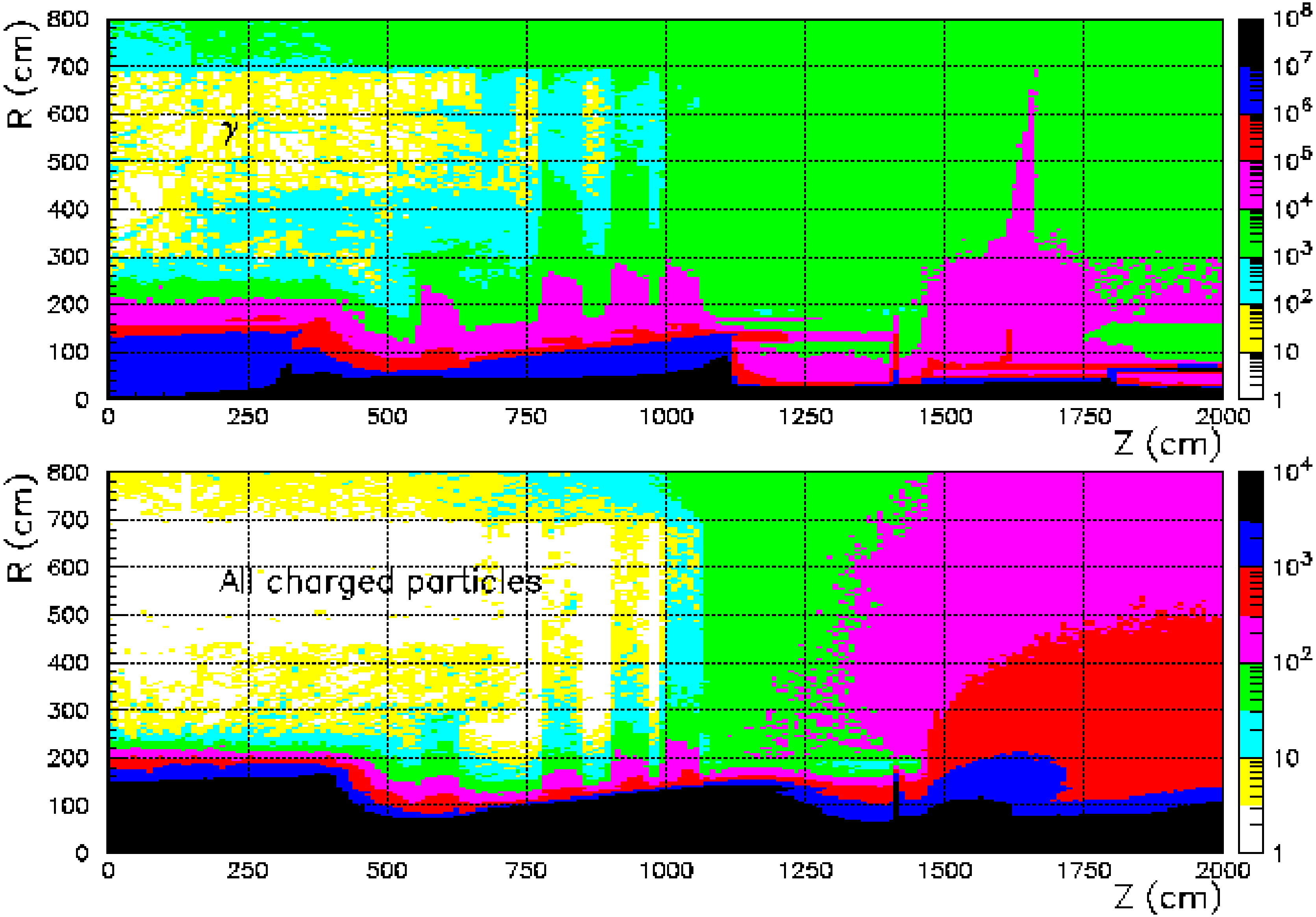
to take responsibility
for this important part
of the CMS Muon System

in collaboration with
Italian and Polish institutes



YOKF: Steel−008
MHLD: Lead
MHUH: Borated Polyethylene
HABC: Hcal average
HAF : Hcal average
FCzS: Thick MagnetiteBoron
FCzF: Thick Steel−008
FCPO: Borated Polyethylene
R (cm)
Z (cm)
EAC : Pb W Oz4
EF1C: Pb W Oz4
QFz1: Thick MagnetiteBoron
QFz0: Thick Steel−008
QUAD: Air
QFz1: Thick MagnetiteBoron
FCzL: Thick Fcal average
QFzC: Thick MagnetiteBoron
QFzF: Thick Magnetite

Neutron originated background



Muon Trigger performance

Basic characteristics

- **minimal p_t threshold**
- **geometrical acceptance**
- **efficiency curves**

Background

- **muon secondaries**
- **punchthrough**
- **neutron bath**

Trigger rates

- **single muon trigger**
- **two muon trigger**
- **cumulative rates**