DAQ for Heavy Ions

Consider Pb-Pb collisions

Assume

- **First Level Trigger rate = 1000 Hz**
- **data: Pixel barrel, 4 outer MSGC and Muons $|\eta|<1.5$, full calorimeters**
- **occupancies — as obtained from simulations** (see next pages)
- **Readout Dual Port Memory (RDPM) input = 200 M Bytes/s**
- **Number of RDPM's = 1000**
- **Switch bandwidth = 500 G bits/s**
- **mass storage capacity = 100 M Bytes/s**

Calculate the data volume for each subdetector

Calculate the data flow

- **from detector Front Ends to Front End Drivers (FED)**
- **from FEDs to RDPMs**
- **through the Switch**

Data volumes for Pb Pb collisions

PIXEL barrel

– 1 module = 2 rows × 8 chips × (64×64) pixels = 65 k pixels

- **Layer 1**
  – (32×10) modules × 65 k pixels = 21 M channels
  – × 4% occupancy = 840 k hits
- **Layer 2**
  – (48×10) modules × 65 k pixels = 32 M channels
  – × 2% occupancy = 630 k hits

Full readout

– 1 channel = analogue information equivalent to 1 Byte
– 53 M channels × 1 Byte = **53 M Bytes**

Zero suppressed readout

– assume readout in blocks: 1 block = 1 module = 65 k pixels
$\Longrightarrow$ 2 Bytes are needed for the address
– 1370 k hits × (1+2) Bytes = **4.1 M Bytes**
– one can reduce it writing cluster center and size instead of each pixel
possible gain ~factor 2 $\Longrightarrow$ data volume ≈ **<u>2 M Bytes</u>**

Data volumes for Pb Pb collisions

***MSGC barrel** (option with all modules 12.5 cm long)*

layer	modules	chips	channels	hits
4 D	57×9=513	×12=6156	×128=788k	×18%=142k
5 S	62×9=558	×8=4464	×128=571k	×14%=80k
6 S	67×9=603	×8=4824	×128=617k	×11%=68k
7 D	72×9=603	×12=7774	×128=995k	×8%=80k
TOTAL			**3 M**	**370 k**

Full readout

- 1 channel = analogue information equivalent to n bits
- 3 M channels × n bits = 3 M bits = n × **371 k Bytes**

Zero suppressed readout

- 370 k hits × 10 bits = 3.7 M bits = **463 k Bytes**

Data volumes for Pb Pb collisions

Muon RPC

– **< 1 k Byte**

Muon Drift Tubes

– **5 k Bytes**

HCAL *(100% occupancy)*

- **full readout**
  – 14616 channels × 10 Bytes = **146 k Bytes**

ECAL *(100% occupancy)*

- **full precise information readout**
  – 3888 towers × 36 crystals × 2 Bytes × 15 time slices = **4.2 M Bytes**
  $\Rightarrow$ *very large data volume, probably 15 time slices not needed (no pileup)*
- **optional - full, 1 time slice readout**
  – 3888 towers × 36 crystals × 2 Bytes = **280 k Bytes**
- **full trigger information readout**
  – strips of 6 crystals, only one time slice
  – 3888 towers × 6 strips × 2 Bytes = **47 k Bytes**

2 Bytes/strip $\Rightarrow$ ***LSB = 50 MeV*** ***Max energy = 3.2 TeV***

Data volumes for Pb Pb collisions

	k Bytes
Pixel barrel	~2000
MSGC barrel	463
ECAL full trigger	47
HCAL full	146
Muon RPC	1
Muon Drift Tubes	5

+ some outer modules of forward MSGC for $|\eta|<1.5$

+ some outer Muon Cathode Strip Chambers for $|\eta|<1.5$

+ VFCAL

3 M Bytes / event

i.e. 3× more than for pp collisions at $L=10^{34} cm^{-2}s^{-1}$.

Assuming (very conservatively) **mass storage of 100 M Bytes/s we can write to tape**

30 events / second

Compressing can give factor ~2 ?, so we hope for

40-60 events / second

or more ...

Data flow for Pb Pb collisions

PIXEL barrel

From Front End to FED

- 1 channel = analogue information equivalent to 8 bits
- 1 link = 4 chips $\times$ (64$\times$64) pixels = 16 k channels
  $\Longrightarrow$ 14 bits are needed for the address

- **Full readout**
  - 16 k channels $\times$ 8 bits $\times$ 1000 Hz = **131 M bits/s**
- **Zero suppressed readout**
  - 16 k channels $\times$ 4% occupancy $\times$ (8+14) bits $\times$ 1000 Hz = **15 M bits/s**

Currently the connection is designed for 3-4 M bits/s expected for pp collisions at L=10^{34}cm^{-2}s^{-1}

Thus we have a bottle-neck at this point !!!

Data flow for Pb Pb collisions

PIXEL barrel **— from FEDs to RDPMs**

– 1 module = 2 rows × 8 chips × (64×64) pixels = 65 536 channels

Layer 1: 16 modules → 1 FED → 1 RDPM

– 16 × 65 536 = 1 M channels

- **Full readout**
  – 1 M channels × 1 Byte × 1000 Hz = **1 G Bytes/s**
- **Zero suppressed readout**
  – 1 M channels × 4% occupancy × 3 Bytes × 1000 Hz = **126 M Bytes/s**

Layer 2: 32 modules → 1 FED → 1 RDPM

– 32 × 65 536 = 2 M channels

- **Full readout**
  – 2 M channels × 1 Byte × 1000 Hz = **2 G Bytes/s**
- **Zero suppressed readout**
  – 2 M channels × 2% occupancy × 3 Bytes × 1000 Hz = **126 M Bytes/s**

⇒ ***zero suppressed option is feasible***

Data flow for Pb Pb collisions

***MSGC barrel** (option with all modules 12.5 cm long)*

- 64 links $\times$ 256 channels = 16 k channels $\rightarrow$ 1 FED
- 8 FEDs $\rightarrow$ 1 RDPM

Full readout

- 8 $\times$ 16 k channels $\times$ 1 bit = 16 k Bytes
- $\times$ 1000 Hz = **16 M Bytes/s**

Zero suppressed readout

- 8 $\times$ 16 k channels $\times$ 18% occupancy $\times$ 10 bits = 30 k Bytes
- $\times$ 1000 Hz = **30 M Bytes/s**

$\Rightarrow$ ***reasonable conditions for both options***

Data flow for Pb Pb collisions

ECAL *(100% occupancy)*

– 64 towers $\rightarrow$ 1 RDPM

- **full precise information readout**
  – 64 towers $\times$ 36 crystals $\times$ 2 Bytes $\times$ 15 time slices = 69 k Bytes
  – $\times$ 1000 Hz = **69 M Bytes/s**

- **optional - full, 1 time slice readout**
  – 64 towers $\times$ 36 crystals $\times$ 2 Bytes = 4.6 k Bytes
  – $\times$ 1000 Hz = **4.6 M Bytes/s**

- **full trigger information readout**
  – strips of 6 crystals, only one time slice
  – 64 towers $\times$ 6 strips $\times$ 2 Bytes = 768 Bytes
  – $\times$ 1000 Hz = **0.8 M Bytes/s**

$\Rightarrow$ ***all options are possible***

Data flow for Pb Pb collisions

HCAL, VFCAL, MUONS

– very low bandwidth required

SWITCH

– event size = 3 M Bytes
– trigger rate = 1000 Hz
$\Longrightarrow$ required bandwidth = **3 G Bytes/s**

– nominal bandwidth = 500 G bits/s = 62 G Bytes/s
– in practice 50% of the nominal bandwidth can be used due to traffic
$\Longrightarrow$ effective bandwidth ≈ **30 G Bytes/s**

$\Rightarrow$ ***large safety margin (factor 10)***

Conclusions

- **No problem with data volume and flow with all detectors, but Pixels**
- **Needed on-line clusterisation of Pixel data**
- **Possible bottle-neck:**
  FE $\rightarrow$ FED rate (15 M bits/s) **higer then for pp** (3-4 M bits/s) !!!

Expected event size (before digital compression)

~ 3 M Bytes

With FLT rate = 1 kHz and mass storage = 100 M Bytes/s one can write

40-60 events / s

depending on the compression factor